1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
B	0000803841	PRODUCTION RELEASED	2009-10-09

SCHEMATIC,MLB,"Kalahari"

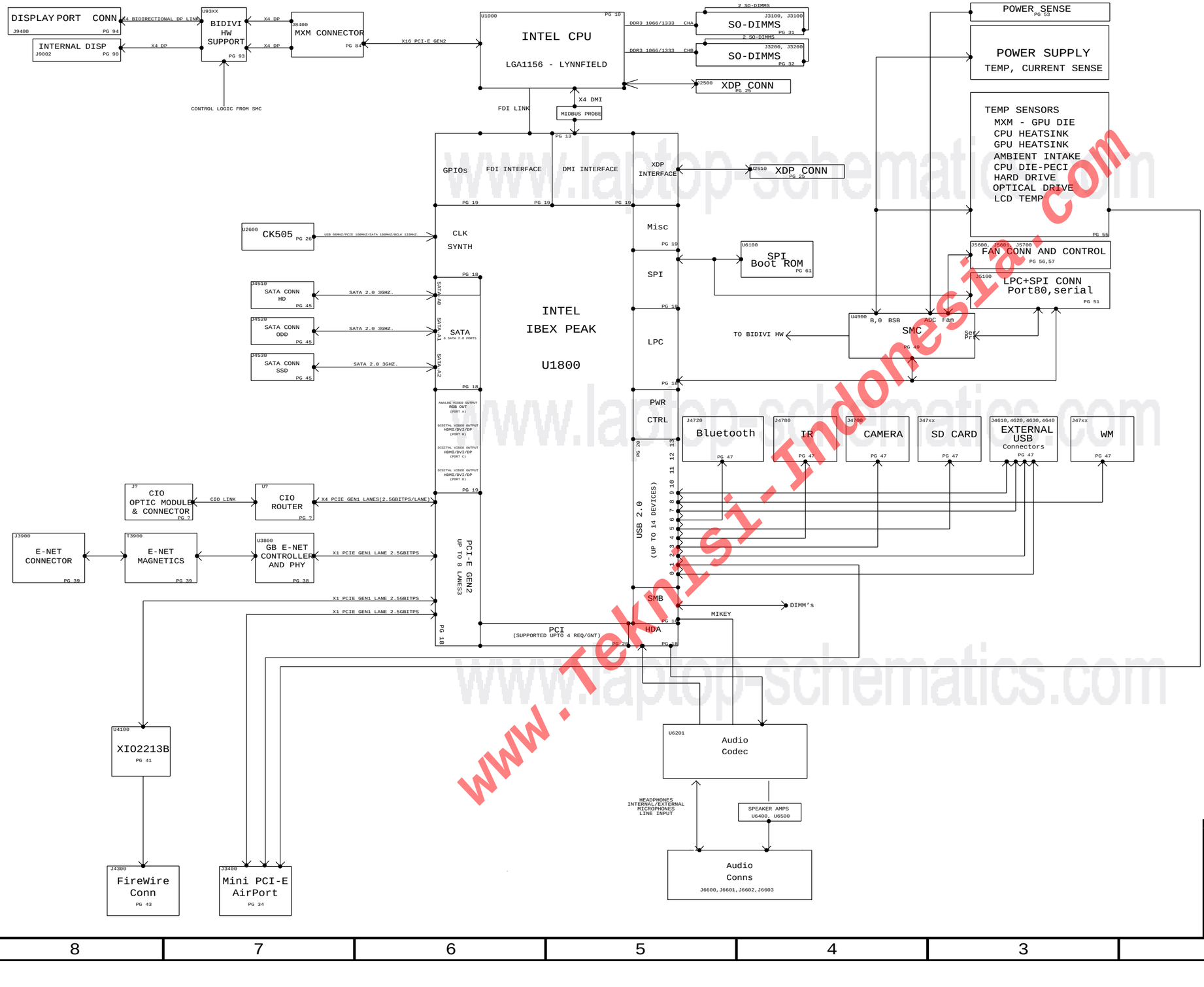
LAST_MODIFIED=Fri Oct 9 15:23:09 2009

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Fri Oct 9 15:23:09 2009

DRAWING TITLE

Apple Inc.

DRAWING NUMBER 051-8233 | SIZE D
REVISION B.0.0
BRANCH
PAGE 1 OF 110
SHEET 1 OF 92



SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE: System Block Diagram

Apple Inc.

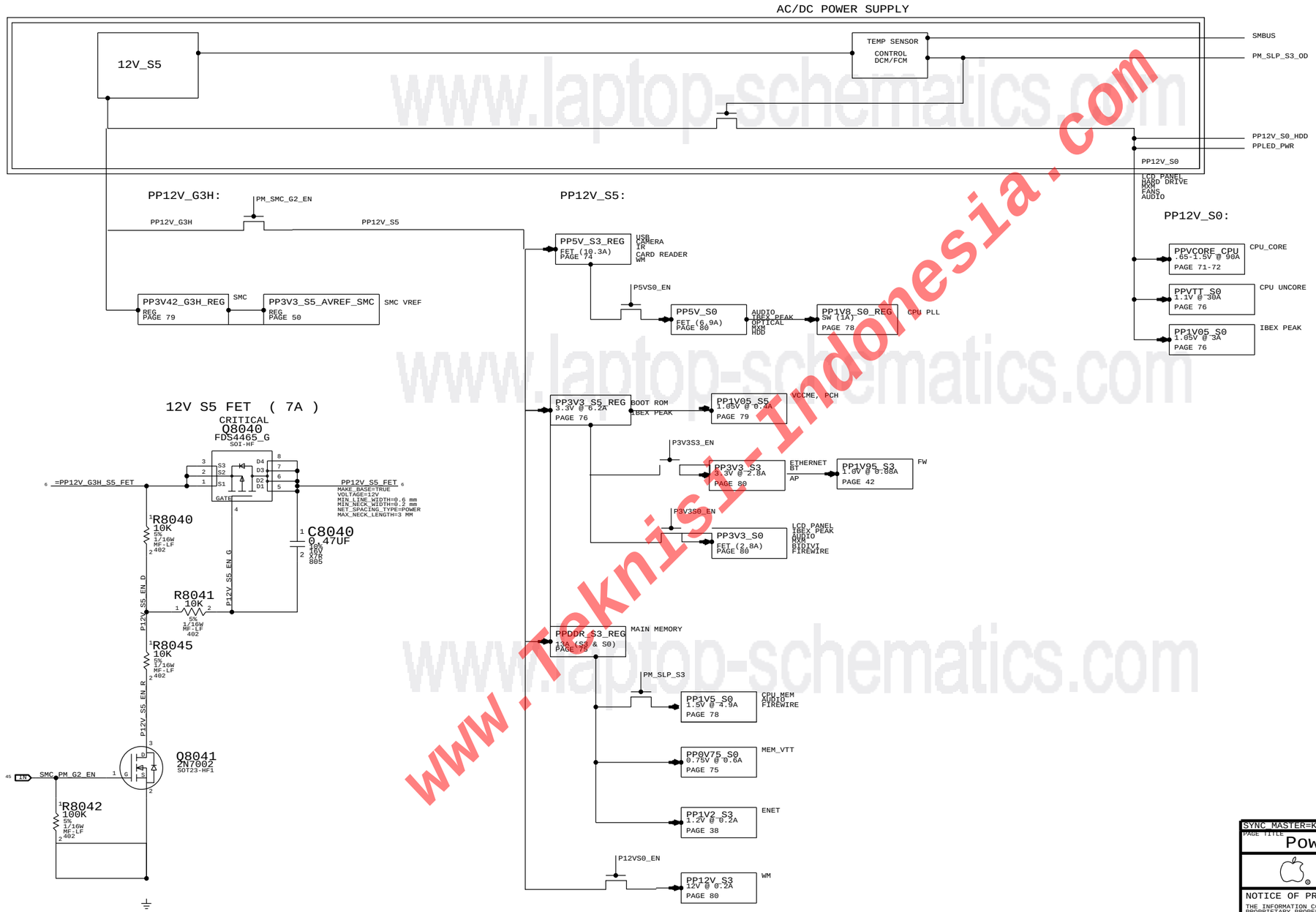
DRAWING NUMBER: 051-8233 SIZE: D

REVISION: B.0.0

BRANCH:

PAGE: 2 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC MASTER=K60 MIKE SYNC DATE=07/01/2009

PAGE TITLE
Power Block Diagram

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

REVISION B.0.0

BRANCH

PAGE 3 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0439	PCBA,MLB,K23F,2.66GHZ	K23F,2P66GHZ_CPU,BASIC,CPUPOC_IMAX_100_120
639-0440	PCBA,MLB,K23F,2.80GHZ	K23F,2P80GHZ_CPU,BASIC,CPUPOC_IMAX_100_120
085-1023	PCBA,MLB,DEV,K23F	DEVELOPMENT,DEV_GROUP

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,XDP,BETTER,MXM,XDP_CPU_BPM,INT_VREF,PCH_VRM,BUF_CLK,PRODUCTION
DEV_GROUP	XDP_CONN,LPCPLUS,MOJOMUX,CPU_TDIODE,MEM_RESET_HW

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S0823	1	IC,IBEX PEAK B3,DESKTOP,FCBGA,PCH,P425	U1800	CRITICAL	
359S0157	1	IC,SLG2AP108,CLK GEN,CK505,QFN3	U2600	CRITICAL	BUF_CLK
341T0211	1	IC,EFI BOOTROM,K23F	U6100	CRITICAL	
338S0765	1	IC,XIO2211ZAY,1394B_PCIE,PHY/LINK	U4100	CRITICAL	
343S0485	1	IC,BCM5764M,68PIN QFN	U3700	CRITICAL	
RAW: 335S0663	1	IC,FLASH,45DB0011D,SOIC-8S1	U3701	CRITICAL	
511S0063	1	SOCKET,LGA1156,CPU-LF	U1000	CRITICAL	
825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3810	1	LFD,SLBLC,PRQ,2.66,95W,1333,B1,8M,LGA	CPU	CRITICAL	2P66GHZ_CPU
337S3811	1	LFD,SLBJJ,PRQ,2.80,95W,1333,B1,8M,LGA	CPU	CRITICAL	2P80GHZ_CPU

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

K23F PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8233	1	SCH,K23F,MLB	SCH1		K23F
820-2733	1	PCBF,K23F,MLB	MLB1		K23F
(338S0489 - BLNK) 341T0212	1	IC,SMC,K23F	U4900	CRITICAL	K23F

SYNC_MASTER=K60_AARON SYNC_DATE=07/01/2009

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

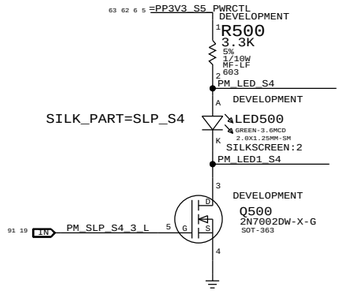
REVISION: B.0.0

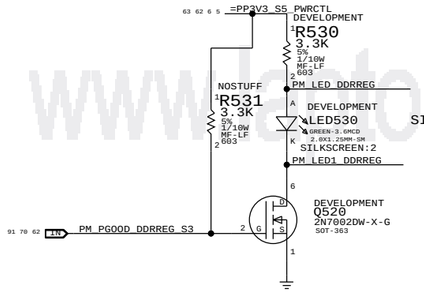
BRANCH:

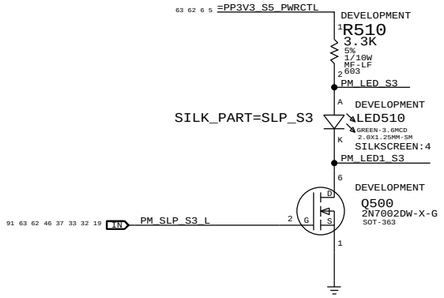
PAGE: 4 OF 110

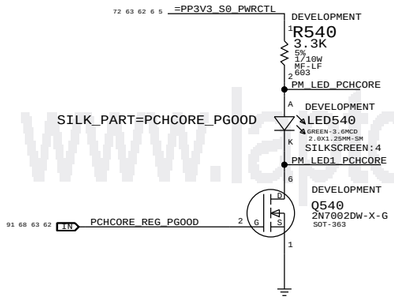
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

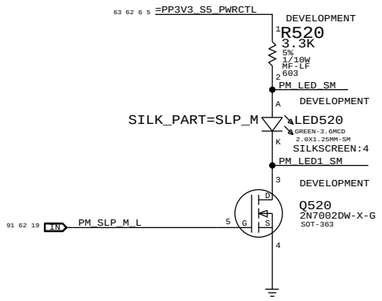
CAN DELETE THESE FOR PROTO1 AND BEYOND

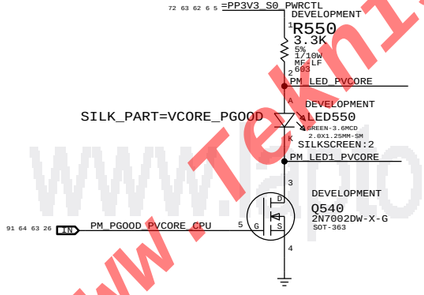












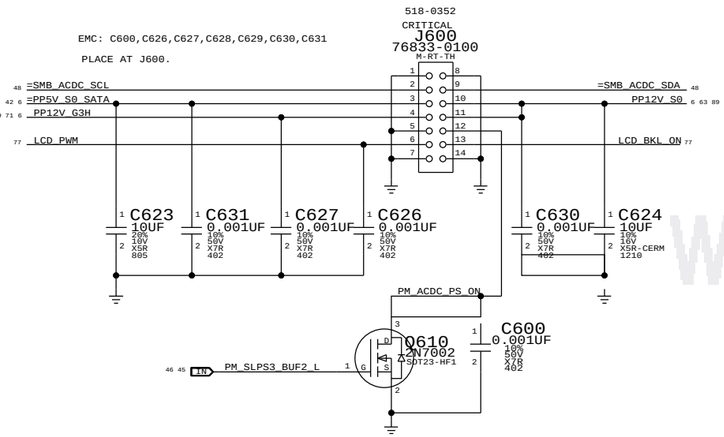
State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

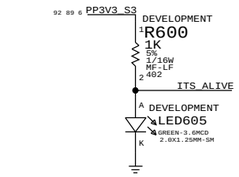
SYNC_MASTER=K60_MIKE SYNC_DATE=07/01/2009

PAGE TITLE
PROTO 0 DEBUG LEDS

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION B.0.0
BRANCH
PAGE 5 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





"S0" RAILS

ONLY ON IN RUN

PPVTT_S0_DDR_FET
- MAKE_BASE=TRUE
- MIN_LINE_WIDTH=0.75V
- MIN_LINE_WIDTH=0.4 mm
- MIN_NECK_WIDTH=0.2 mm
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

=PP0V75_S0_MEM_VTT_B
=PP0V75_S0_MEM_VTT_A

PPVCORE_S0_CPU
- MAKE_BASE=TRUE
- VOLTAGE=1.1V
- MIN_LINE_WIDTH=0.6MM
- MIN_NECK_WIDTH=0.3MM
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

=PPVCORE_S0_CPU_REG
=PPVCORE_S0_CPU

PPVTT_S0_CPU
- MAKE_BASE=TRUE
- VOLTAGE=1.1V
- MIN_LINE_WIDTH=0.6 mm
- MIN_NECK_WIDTH=0.2 mm
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

=PPVTT_S0_CPU

PPVTT_S0
- MAKE_BASE=TRUE
- VOLTAGE=1.1V
- MIN_LINE_WIDTH=0.6 mm
- MIN_NECK_WIDTH=0.2 mm
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

=PPVTT_S0_CPU_REG
=PPVTT_S0_PCH_VCC_DMI
=PPVTT_S0_XDP
=PPVTT_S0_PCH_VCCP_CPU

PP1V5_CPU_MEM
- MAKE_BASE=TRUE
- VOLTAGE=1.5V
- MIN_LINE_WIDTH=0.4MM
- MIN_NECK_WIDTH=0.2MM
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

=PP1V5_CPU_MEM

PP1V5_S0
- MAKE_BASE=TRUE
- VOLTAGE=1.5V
- MIN_LINE_WIDTH=0.4MM
- MIN_NECK_WIDTH=0.2MM
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PP1V5_S0_FET
=PP1V5_S0_AUD_DIG
=PP1V5_FWRS0_FWXIO
=PP1V5_S0_CK505

PP1V8_S0_CPU
- MAKE_BASE=TRUE
- VOLTAGE=1.8V
- MIN_LINE_WIDTH=0.4MM
- MIN_NECK_WIDTH=0.2MM
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

=PP1V8_S0_CPU_PLL

PP1V8_S0
- MAKE_BASE=TRUE
- VOLTAGE=1.5V
- MIN_LINE_WIDTH=0.4MM
- MIN_NECK_WIDTH=0.2MM
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PP1V8_S0_REG
=PP3V3R1V8_S0_PCH_VCCPNAND
=PP1V8R1V5_S0_PCH_VCCVRM

PPVAXG_S0_CPU
- MAKE_BASE=TRUE
- VOLTAGE=0V
- MIN_LINE_WIDTH=0.6MM
- MIN_NECK_WIDTH=0.3MM
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

=PPVAXG_S0_CPU

PP3V3_S0
- MAKE_BASE=TRUE
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.4MM
- MIN_NECK_WIDTH=0.2MM
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PP3V3_S0_FET
=PP3V3_S0_PCH
=PP3V3_S0_FAN
=PP3V3_S0_PCH_VCCADAC
=PPSPD_S0_MEM_A
=PPSPD_S0_MEM_B
=PP3V3_S0_VRD
=PP3V3_S0_AUDIO
=PP3V3R1V5_S0_PCH_VCCSUSHDA
=PP3V3_S0_SMBUS
=PP3V3_S0_SMC_LS
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_SMBUS_SMC_B_S0
=PP3V3_S0_SMBUS_SMC_MGMT
=PP3V3_S0_DPCONN
=PP3V3_S0_TSENS
=PP3V3_S0_MXM
=PP3V3_S0_XDP
=PP3V3_S0_ODD
=PP3V3_S0_SATALED
=PP3V3_S0_SMC
=PP3V3_S0_PWRCTL
=PP3V3_S0_PCH_VCC3_3_CORE
=PP3V3_S0_VIDEO
=PP3V3_FW_FWPHY
=PP3V3_FWRS0_FWXIO
=PP3V3_S0_DP
=PP3V3_S0_PCH_VCC3_3_PCI
=PP3V3_S0_CK505
=PP3V3_S0_PCH_GPIO
=PP3V3_S0_PCH_STRAPS
=PP3V3_S0_PCH_VCC3_3_SATA
=PP3V3_S0_RSTBUF
=PP3V3_S0_ME
=PP3V3_S0_ENET
=PP3V3_S0_PCH_PM
=PP3V3_S0_SMBUS_SMC_BSA

PP5V_S0
- MAKE_BASE=TRUE
- VOLTAGE=5V
- MIN_LINE_WIDTH=0.5 mm
- MIN_NECK_WIDTH=0.2 mm
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PP5V_S0_FET
=PP5V_S0_AUDIO
=PP5V_S0_SATA
=PP5V_S0_MXM
=PP5V_S0_VRD
=PP5V_S0_ISENSE
=PP5V_S0_P1V8_VREG
=PP5V_S0_PCH
=PP5V_S0_CPU_VTT_VREG
=PP5V_S0_LPCPLUS
=PP5V_S0_PCH_CORE_VREG

PP1V05_S0
- MAKE_BASE=TRUE
- VOLTAGE=1.05V
- MIN_LINE_WIDTH=0.6 mm
- MIN_NECK_WIDTH=0.2 mm
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PP1V05_S0_REG
=PP1V05_S0_PCH_VCCADPLL
=PP1V05_S0_PCH_VCCIO_DMI
=PP1V05_S0_PCH
=PP1V05_S0_SM_FET
=PP1V05_S0_PCH_VCCIO_SATA
=PP1V05_S0_PCH_VCCIO_PCIE
=PP1V05_S0_PCH_VCC_CORE
=PP1V05_S0_PCH_VCCIO_USB
=PP1V05_S0_CK505

PP1V05_SM_PCH_LAN
- MAKE_BASE=TRUE
- VOLTAGE=1.05V
- THIS NET IS NOT CONNECTED TO ANY VOLTAGE RAIL. INSTEAD ON PAGE 24 IT IS CONNECTED TO GND THROUGH A RESISTOR

=PP1V05_SM_PCH_VCC_LAN

PP0V75_S0
- MAKE_BASE=TRUE
- VOLTAGE=0.75V
- MIN_LINE_WIDTH=0.4 mm
- MIN_NECK_WIDTH=0.2 mm
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PPVTT_S0_DDR_LDO
=PP0V75_S0_MEM_VTT_S0FET

PP12V_S0
- MAKE_BASE=TRUE
- VOLTAGE=12V
- MIN_LINE_WIDTH=0.5 mm
- MIN_NECK_WIDTH=0.25 mm
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

=PP12V_S0_FAN
=PP12V_S0_AUDIO_SPKRAMP
=PP12V_S0_VRD
=PPV_S0_MXM_PWR
=PP12V_S0_LCD
=PP12V_S0_PCH_CORE_VREG
=PP12V_S0_CPU_VTT_VREG
=PP12V_S0_PWRCTL

"S3" RAILS

ON IN RUN AND SLEEP

PP1V5_S3
- MAKE_BASE=TRUE
- VOLTAGE=1.5V
- MIN_LINE_WIDTH=0.6 mm
- MIN_NECK_WIDTH=0.2 mm
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PP1V5_S3_REG
=PP1V5_S3_MEMRESET
=PPDDR_S3_S0FET
=PP1V5_S3_MEM_A
=PP1V5_S3_MEM_B

PP12V_S3
- MAKE_BASE=TRUE
- VOLTAGE=12V
- MIN_LINE_WIDTH=0.6 mm
- MIN_NECK_WIDTH=0.2 mm
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PP12V_S3_FET
=PP12V_S3_WM

PP3V3_S3
- MAKE_BASE=TRUE
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.5 mm
- MIN_NECK_WIDTH=0.2 mm
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PP3V3_S3_FET
=PP3V3_S3_VREFMRGN
=PP3V3_S3_BT
=PP3V3_S3_PCH_STRAPS
=PP3V3_S3_SDCARD
=PP3V3_S3_SMBUS_SMC_A_S3
=PP3V3_S3_MINI
=PP3V3_S3_PWRCTL
=PP3V3_S3_WM
=PP3V3_S3_SMBUS
=PP3V3_S3_MEMRESET
=PP3V3_S3_BRCRYPT
=PP3V3_S3_ENET
=PP3V3_S3_USB_HUB
=PP3V3_S3_USB_RESET

PP5V_S3
- MAKE_BASE=TRUE
- VOLTAGE=5V
- MIN_LINE_WIDTH=0.6MM
- MIN_NECK_WIDTH=0.2MM
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PP5V_S3_REG
=PP5V_S3_USB
=PP5V_S3_S0FET
=PP5V_S3_CAMERA
=PP5V_S3_IR
=PP5V_S3_VREFMRGN
=PP5V_S3_PWRCTL
=PP5V_S3_MEMRESET
=PP5V_S3_DDR_VREG
=PP5V_S3_BRAY

PP3V3_S0M
- MAKE_BASE=TRUE
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.5 mm
- MIN_NECK_WIDTH=0.2 mm
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PP3V3_SM_FET
=PP3V3_SM_PCH_VCC_ME
=PP3V3_SM_PWRCTL

PP1V05_SM
- MAKE_BASE=TRUE
- VOLTAGE=1.05V
- MIN_LINE_WIDTH=0.6 mm
- MIN_NECK_WIDTH=0.2 mm
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PP1V05_SM_FET
=PP1V05_SM_PCH_VCC_ME
=PP1V05_SM_ME

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN S5

PP1V05_S5
- MAKE_BASE=TRUE
- VOLTAGE=1.05V
- MIN_LINE_WIDTH=0.5 mm
- MIN_NECK_WIDTH=0.2 mm
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PP1V05_S5_REG
=PP1V05_S5_SM_FET

PP3V3_S5
- MAKE_BASE=TRUE
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.6MM
- MIN_NECK_WIDTH=0.2MM
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PP3V3_S5_REG
=PP3V3_S5_PCH
=PP3V3_S5_PCH_GPIO
=PP3V3_S5_ROM
=PP3V3_S5_PCH_VCCSUS3_3_USB
=PP3V3_S5_PWRCTL
=PP3V3_S5_S3FET
=PP3V3_S5_S0FET
=PP3V3_S5_P1V05S5_VREG
=PP3V3_S5_SM_FET
=PP3V3_S5_PCH_STRAPS
=PP3V3_S5_CPURESET
=PP3V3_S5_XDP
=PP3V3_S5_MEMRESET
=PP3V3_S5_LPCPLUS

PP5V_S5
- MAKE_BASE=TRUE
- VOLTAGE=5V
- MIN_LINE_WIDTH=0.4 MM
- MIN_NECK_WIDTH=0.2 mm
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PP5V_S5_LDO
=PP5V_S5_PCH

PP12V_S5
- MAKE_BASE=TRUE
- VOLTAGE=12V
- MIN_LINE_WIDTH=0.6 mm
- MIN_NECK_WIDTH=0.2 mm
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PP12V_S5_FET
=PP12V_S5_DDR_VREG
=PP12V_S5_P3V3S5_VREG
=PP12V_S5_P5VS3_VREG
=PP12V_S5_S3_FET
=PP12V_S5_PWRCTL
=PP12V_S5_FW

"G3H" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN G3HOT PER SMC

G3H: ALIASES

PP3V42_G3H
- MAKE_BASE=TRUE
- VOLTAGE=3.42V
- MIN_LINE_WIDTH=0.6MM
- MIN_NECK_WIDTH=0.2MM
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

PP3V42_G3H_REG
=PP3V3_S5_RTC_D
=PP3V3_G3H_SMC
=PP3V3_G3H_SMCUSBMUX
=PP3V42_G3H_AVREF
=PP3V3_G3H_LPCPLUS

PP12V_G3H
- MAKE_BASE=TRUE
- VOLTAGE=12V
- MIN_LINE_WIDTH=0.6 mm
- MIN_NECK_WIDTH=0.4 mm
- NET_SPACING_TYPE=POWER
- MAX_NECK_LENGTH=3 MM

=PP12V_G3H_S5_FET

GND RAILS

GND
- MIN_LINE_WIDTH=0.6MM
- MIN_NECK_WIDTH=0.2MM
- VOLTAGE=0V
- NET_SPACING_TYPE=GND
- MAKE_BASE=TRUE
- MAX_NECK_LENGTH=4.1 MM

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

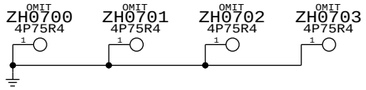
PAGE TITLE: Power Conn / Alias

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D
REVISION: B.0.0
BRANCH:
PAGE: 6 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CPU Heatsink

4mm Plated Holes (998-0850)

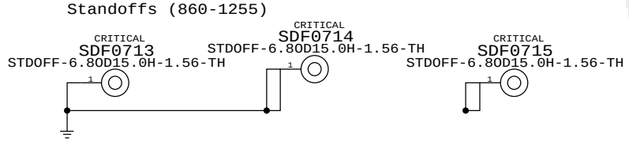


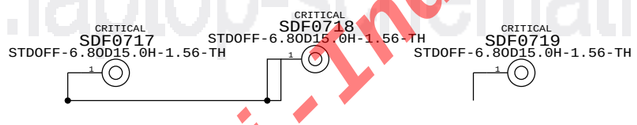
PCH HEATSINK

EMC Springs (870-1125) Removed 2009-10-05

Rear Cover

Standoffs (860-1255)





Backer Plate

Nuts (835-0269)

For EMC

EMC Spring (870-1577); Near DIMMs

EMC POGO Pins (870-1698); Near DIMMs

DIMM CONNECTOR NUTS

Nuts (805-9582)

SYNC MASTER=K60 SIJI SYNC DATE=07/01/2009

PAGE TITLE: Holes

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

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SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

UNUSED CPU SIGNALS

TP_CPU_RSVD<41..29>	=	NC_CPU_RSVD<41..29>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_CPU_RSVD<26..1>	=	NC_CPU_RSVD<26..1>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_CPU_FC_AE38	=	NC_CPU_FC_AE38	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_CPU_FC_AG40	=	NC_CPU_FC_AG40	MAKE_BASE=TRUE	NO_TEST=TRUE

NC ON UNUSED PCI ALIASES

TP_PCI_AD<31..0>	=	NC_PCI_AD<31..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_PCI_C_BE_L<3..0>	=	NC_PCI_C_BE_L<3..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_PCI_PAR	=	NC_PCI_PAR	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_PCI_RESET_L	=	NC_PCI_RESET_L	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_PCIE_CLK100M_XDPP	=	NC_PCIE_CLK100M_XDPP	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_PCIE_CLK100M_XDPN	=	NC_PCIE_CLK100M_XDPN	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DMI_CLK100M_LAP	=	NC_DMI_CLK100M_LAP	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DMI_CLK100M_LAN	=	NC_DMI_CLK100M_LAN	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_LPC_DREQ1_L	=	NC_LPC_DREQ1_L	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_LPC_DREQ0_L	=	NC_LPC_DREQ0_L	MAKE_BASE=TRUE	NO_TEST=TRUE

NC ON UNUSED NAND ALIASES

TP_NV_CE_L<3..0>	=	NC_NV_CE_L<3..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_NV_DQS<1..0>	=	NC_NV_DQS<1..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_NV_DQ<15..0>	=	NC_NV_DQ<15..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_NV_RB_L	=	NC_NV_RB_L	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_NV_WR_RE_L<1..0>	=	NC_NV_WR_RE_L<1..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_NV_WE_CK_L<1..0>	=	NC_NV_WE_CK_L<1..0>	MAKE_BASE=TRUE	NO_TEST=TRUE

NC ON UNUSED MISC ALIASES

TP_JTAG_XDP_TRST_L	=	NC_JTAG_XDP_TRST_L	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_PCH_PWM0	=	NC_PCH_PWM0	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_PCH_PWM1	=	NC_PCH_PWM1	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_PCH_PWM2	=	NC_PCH_PWM2	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_PCH_PWM3	=	NC_PCH_PWM3	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_PCH_SST	=	NC_PCH_SST	MAKE_BASE=TRUE	NO_TEST=TRUE

NC ON UNUSED MEM ALIASES

TP_MEM_A_CS_L<7..4>	=	NC_MEM_A_CS_L<7..4>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_MEM_A_DQ_CB<7..0>	=	NC_MEM_A_DQ_CB<7..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_MEM_A_DQS_N<8>	=	NC_MEM_A_DQS_N<8>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_MEM_A_DQS_P<8>	=	NC_MEM_A_DQS_P<8>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_MEM_B_CS_L<7..4>	=	NC_MEM_B_CS_L<7..4>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_MEM_B_DQ_CB<7..0>	=	NC_MEM_B_DQ_CB<7..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_MEM_B_DQS_N<8>	=	NC_MEM_B_DQS_N<8>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_MEM_B_DQS_P<8>	=	NC_MEM_B_DQS_P<8>	MAKE_BASE=TRUE	NO_TEST=TRUE

TP_PCI_T28_D2R_N<3..0>	=	NC_PCI_T28_D2R_N<3..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_PCI_T28_D2R_P<3..0>	=	NC_PCI_T28_D2R_P<3..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_PCI_T28_R2D_C_N<3..0>	=	NC_PCI_T28_R2D_C_N<3..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_PCI_T28_R2D_C_P<3..0>	=	NC_PCI_T28_R2D_C_P<3..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_HDA_SDIN1	=	NC_HDA_SDIN1	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_HDA_SDIN2	=	NC_HDA_SDIN2	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_HDA_SDIN3	=	NC_HDA_SDIN3	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_PCIE_CLK100M_PE5P	=	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_PCIE_CLK100M_PE5N	=	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_NV_RCOMP	=	NC_NV_RCOMP	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_CLK100M_EXCARD_P	=	NC_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_CLK100M_EXCARD_N	=	NC_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_7N	=	NC_USB_7N	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_7P	=	NC_USB_7P	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_6N	=	NC_USB_6N	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_6P	=	NC_USB_6P	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_1N	=	NC_USB_1N	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_1P	=	NC_USB_1P	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_3N	=	NC_USB_3N	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_3P	=	NC_USB_3P	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_5N	=	NC_USB_5N	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_5P	=	NC_USB_5P	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_9N	=	NC_USB_9N	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_9P	=	NC_USB_9P	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_10N	=	NC_USB_10N	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_10P	=	NC_USB_10P	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_11N	=	NC_USB_11N	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_11P	=	NC_USB_11P	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_12N	=	NC_USB_12N	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_12P	=	NC_USB_12P	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_13N	=	NC_USB_13N	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_USB_13P	=	NC_USB_13P	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_EXCARD_D2R_P	=	NC_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_EXCARD_D2R_N	=	NC_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_EXCARD_R2D_C_P	=	NC_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=TRUE
PCIE_EXCARD_R2D_C_N	=	NC_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SDVO_TVCLKINN	=	NC_SDVO_TVCLKINN	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SDVO_TVCLKINP	=	NC_SDVO_TVCLKINP	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SDVO_STALLN	=	NC_SDVO_STALLN	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SDVO_STALLP	=	NC_SDVO_STALLP	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SDVO_INTN	=	NC_SDVO_INTN	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SDVO_INTP	=	NC_SDVO_INTP	MAKE_BASE=TRUE	NO_TEST=TRUE

NC ON UNUSED SATA ALIASES

TP_SATA_D_D2RN	=	NC_SATA_D_D2RN	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SATA_D_D2RP	=	NC_SATA_D_D2RP	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SATA_D_R2D_CN	=	NC_SATA_D_R2D_CN	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SATA_D_R2D_CP	=	NC_SATA_D_R2D_CP	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SATA_E_D2RN	=	NC_SATA_E_D2RN	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SATA_E_D2RP	=	NC_SATA_E_D2RP	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SATA_E_R2D_CN	=	NC_SATA_E_R2D_CN	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SATA_E_R2D_CP	=	NC_SATA_E_R2D_CP	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SATA_F_D2RN	=	NC_SATA_F_D2RN	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SATA_F_D2RP	=	NC_SATA_F_D2RP	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SATA_F_R2D_CN	=	NC_SATA_F_R2D_CN	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_SATA_F_R2D_CP	=	NC_SATA_F_R2D_CP	MAKE_BASE=TRUE	NO_TEST=TRUE

NC ON UNUSED DISPLAY ALIASES

TP_CRT_IG_DDC_CLK	=	NC_CRT_IG_DDC_CLK	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_CRT_IG_DDC_DATA	=	NC_CRT_IG_DDC_DATA	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_CRT_IG_RED	=	NC_CRT_IG_RED	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_CRT_IG_GREEN	=	NC_CRT_IG_GREEN	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_CRT_IG_BLUE	=	NC_CRT_IG_BLUE	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_CRT_IG_HSYNC	=	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_CRT_IG_VSYNC	=	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_B_MLN<3..0>	=	NC_DP_IG_B_MLN<3..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_B_MLP<3..0>	=	NC_DP_IG_B_MLP<3..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_B_AUX_N	=	NC_DP_IG_B_AUXN	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_B_AUX_P	=	NC_DP_IG_B_AUXP	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_B_HPD	=	NC_DP_IG_B_HPD	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_B_DDC_CLK	=	NC_DP_IG_B_CTRL_CLK	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_B_DDC_DATA	=	NC_DP_IG_B_CTRL_DATA	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_C_MLN<3..0>	=	NC_DP_IG_C_MLN<3..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_C_MLP<3..0>	=	NC_DP_IG_C_MLP<3..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_C_AUX_N	=	NC_DP_IG_C_AUXN	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_C_AUX_P	=	NC_DP_IG_C_AUXP	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_C_HPD	=	NC_DP_IG_C_HPD	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_C_CTRL_CLK	=	NC_DP_IG_C_CTRL_CLK	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_C_CTRL_DATA	=	NC_DP_IG_C_CTRL_DATA	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_D_MLN<3..0>	=	NC_DP_IG_D_MLN<3..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_D_MLP<3..0>	=	NC_DP_IG_D_MLP<3..0>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_D_AUXN	=	NC_DP_IG_D_AUXN	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_D_AUXP	=	NC_DP_IG_D_AUXP	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_D_HPD	=	NC_DP_IG_D_HPD	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_D_CTRL_CLK	=	NC_DP_IG_D_CTRL_CLK	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_DP_IG_D_CTRL_DATA	=	NC_DP_IG_D_CTRL_DATA	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_GFX_VID<0..6>	=	NC_GFX_VID<0..6>	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_GFX_VSENSE_N	=	NC_GFX_VSENSE_N	MAKE_BASE=TRUE	NO_TEST=TRUE
TP_GFX_VSENSE_P	=	NC_GFX_VSENSE_P	MAKE_BASE=TRUE	NO_TEST=TRUE

SYNC MASTER=K60 SIJI SYNC DATE=07/01/2009

PAGE TITLE

UNUSED SIGNAL ALIAS

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PEG Slot Support

THIS SIGNAL NAME IS CONNECTED TO MXM

18 IN PEG_CLK100M_P — 84 — GPU_CLK100M_PCIE_P — CLK_100M_MXM_P — OUT 73
MAKE_BASE=TRUE

18 IN PEG_CLK100M_N — 84 — GPU_CLK100M_PCIE_N — CLK_100M_MXM_N — OUT 73
MAKE_BASE=TRUE

10 IN =PEG_R2D_C_P<0..15> — PEG_R2D_C_P<0..15> — OUT 75 84
MAKE_BASE=TRUE

10 IN =PEG_R2D_C_N<0..15> — PEG_R2D_C_N<0..15> — OUT 75 84
MAKE_BASE=TRUE

10 OUT =PEG_D2R_P<0..15> — PEG_D2R_P<0..15> — IN 75 84
MAKE_BASE=TRUE

10 OUT =PEG_D2R_N<0..15> — PEG_D2R_N<0..15> — IN 75 84
MAKE_BASE=TRUE

18 IN PEG_CLKREQ_L — MXM_CLKREQ_L — OUT 73
MAKE_BASE=TRUE

73 MXM_RESET_L — PEG_RESET_L — 27 91
MAKE_BASE=TRUE

91 85 19 IN PM_CLK32K_SUSCLK_R — R929 22 5% 1/16W MF-LF 402 — PM_CLK32K_SUSCLK — OUT 45 85 91
PLACEMENT_NOTE=PLACE CLOSE TO U1800

SYNC MASTER=K60_SIJI SYNC DATE=07/01/2009

PAGE TITLE: Signal Aliases

Apple Inc.

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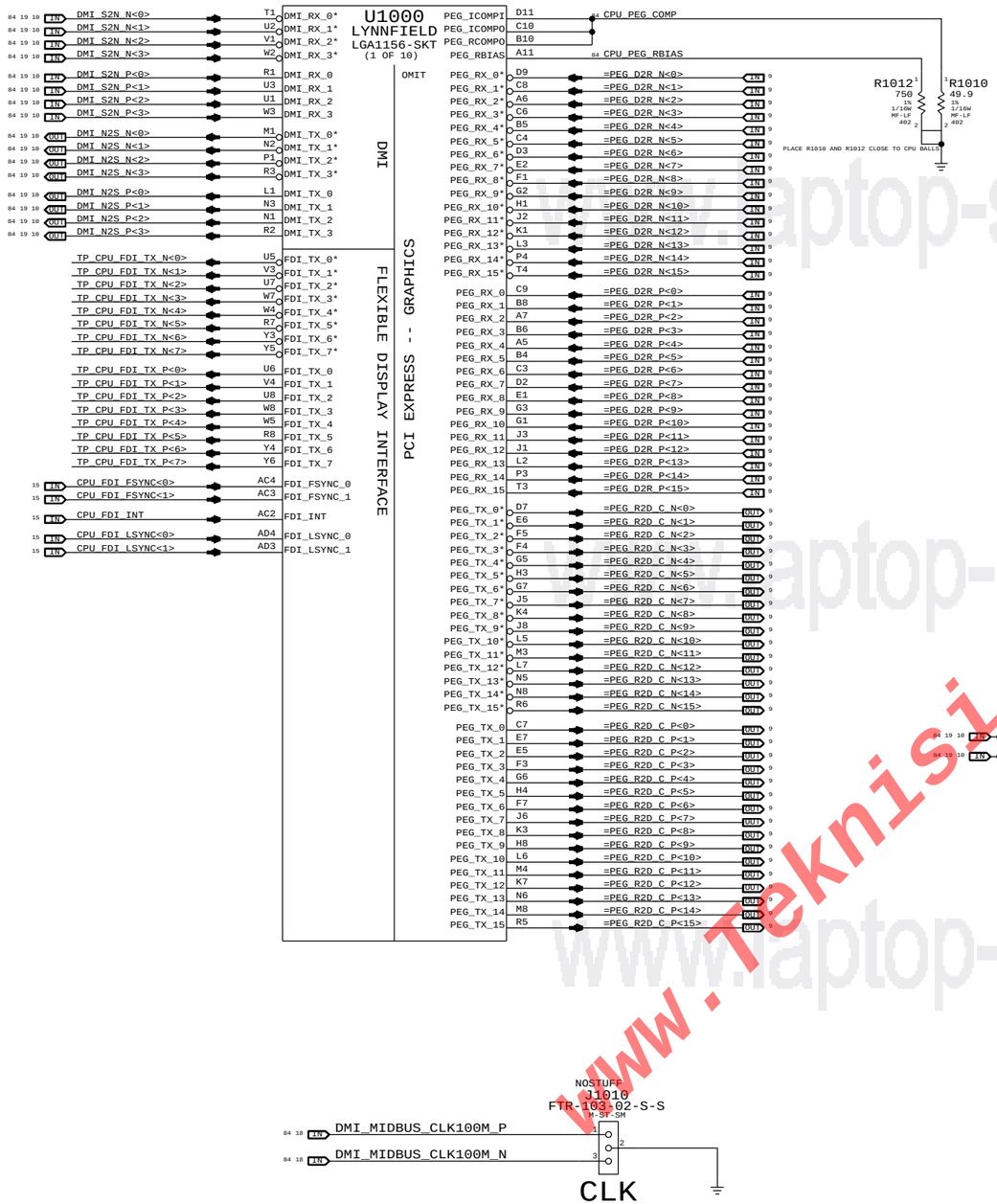
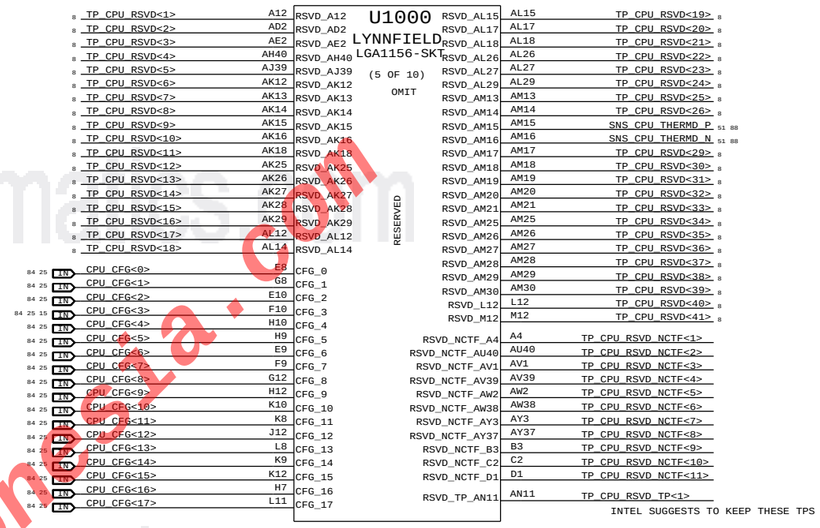
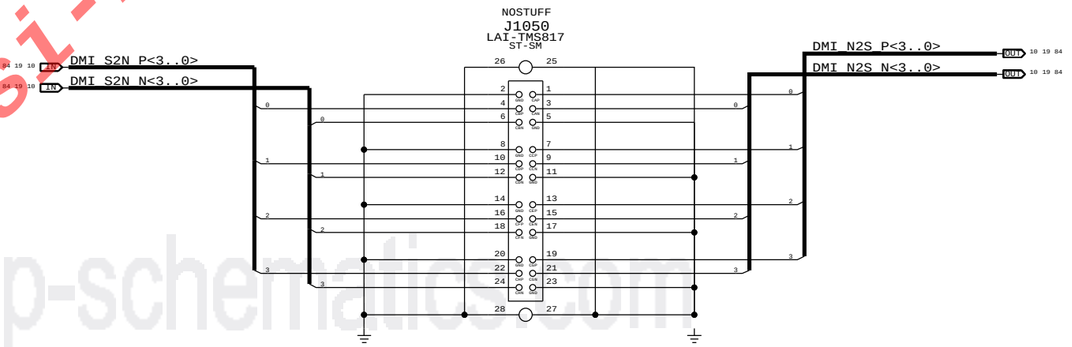
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





FOR LYNNFIELD PROCESSOR
CFG [1:0] :PCIE CONFIGURATION SELECT 11 = 1 X16 PCI EXPRESS 10 = 2 X8 PCI EXPRESS
FOR CLARKDALE PROCESSOR
CFG3 :PCIE LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG4 :NOT USED ON DESKTOP



PAGE TITLE: CPU DMI/PEG/FDI/RSVD

Apple Inc.

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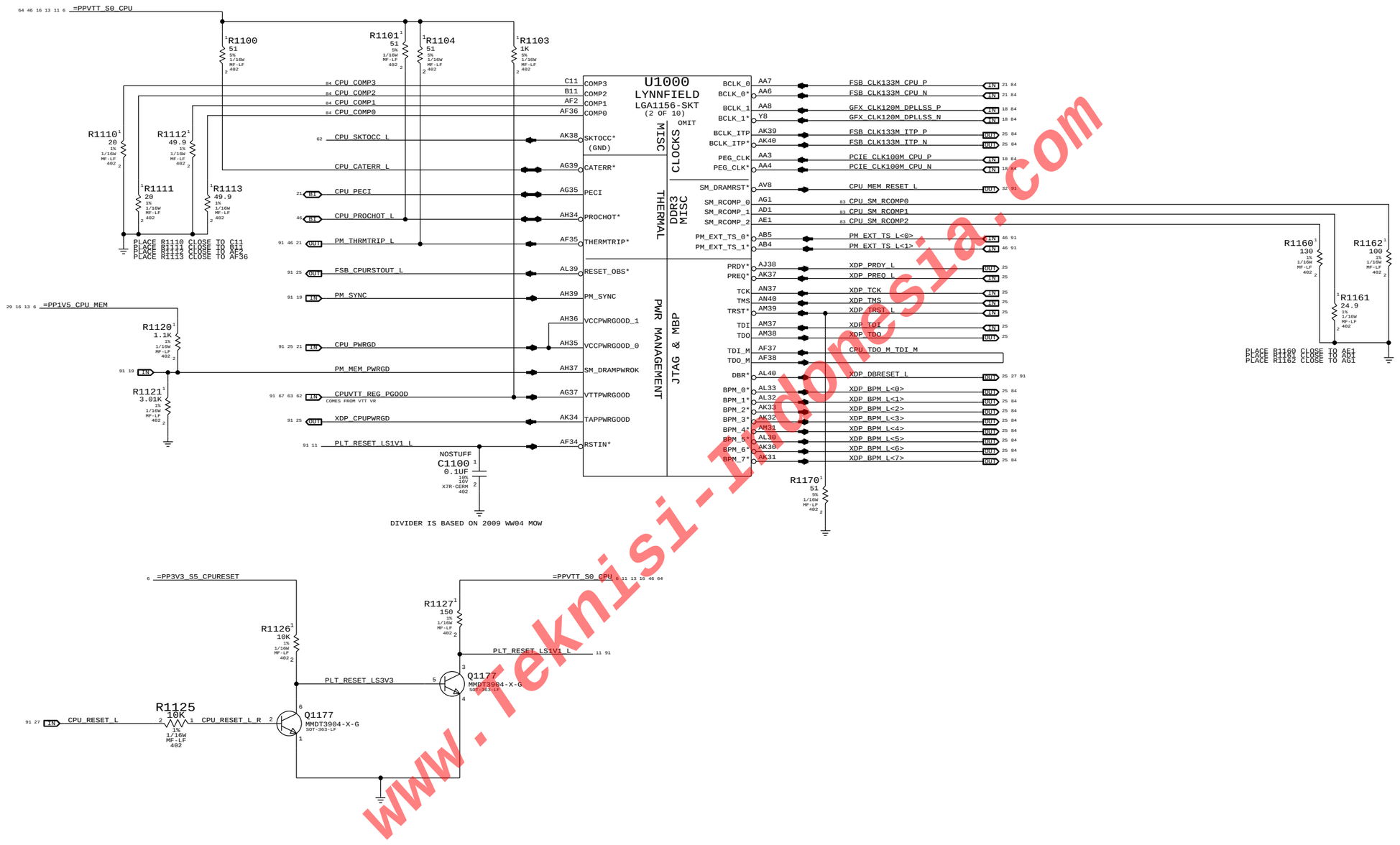
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



PAGE TITLE
CPU CLOCK/MISC/JTAG

Apple Inc.

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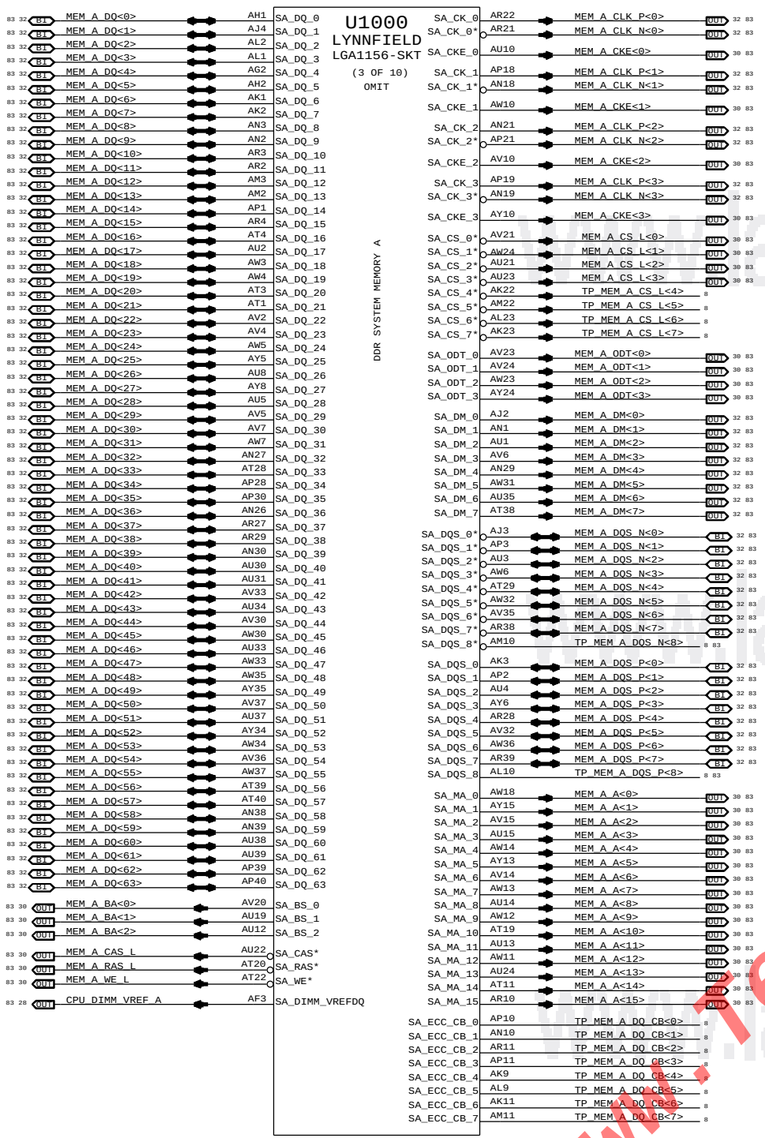

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

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=PPVCORE_S0_CPU 6 13 16

U1000
LYNNFIELD
LGA1156-SKT
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OMIT

VCC

J21	VCC_100	
J22	VCC_101	
J24	VCC_102	
J25	VCC_103	
J27	VCC_104	
J28	VCC_105	
J30	VCC_106	
J31	VCC_107	
J33	VCC_108	
J34	VCC_109	
J36	VCC_110	
J37	VCC_111	
J39	VCC_112	
J40	VCC_113	
K17	VCC_114	
K18	VCC_115	
K20	VCC_116	
K21	VCC_117	
K23	VCC_118	
K24	VCC_119	
K26	VCC_120	
K27	VCC_121	
K29	VCC_122	
K30	VCC_123	
K32	VCC_124	
K33	VCC_125	
K35	VCC_126	
K36	VCC_127	
K38	VCC_128	
K39	VCC_129	
L17	VCC_130	
L19	VCC_131	
L20	VCC_132	
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L28	VCC_137	
L29	VCC_138	
L31	VCC_139	
L32	VCC_140	
L34	VCC_141	
L35	VCC_142	
L37	VCC_143	
L38	VCC_144	
L40	VCC_145	
M17	VCC_146	
M19	VCC_147	
M21	VCC_148	
M22	VCC_149	
M24	VCC_150	
M25	VCC_151	
M27	VCC_152	
M28	VCC_153	
M30	VCC_154	
M33	VCC_155	
M34	VCC_156	
M36	VCC_157	
M37	VCC_158	
M39	VCC_159	
M40	VCC_160	
N33	VCC_161	
N35	VCC_162	
N36	VCC_163	
N38	VCC_164	
N39	VCC_165	
P33	VCC_166	
P34	VCC_167	
P35	VCC_168	
P36	VCC_169	
P37	VCC_170	
P38	VCC_171	
P39	VCC_172	
R40	VCC_173	
R33	VCC_174	
R34	VCC_175	
R35	VCC_176	
R36	VCC_177	
R37	VCC_178	
R38	VCC_179	
R39	VCC_180	
R40	VCC_181	

NCTF

CGC_TP_NCTF	B39	TP_CPU_CGC_NCTF
VCC_NCTF_0	A38	=PPVCORE_S0_CPU 6 13 16
VCC_NCTF_1	C40	
FC_AE38	AE38	TP_CPU_FC_AE38 8
FC_AG40	AG40	TP_CPU_FC_AG40 8

16 13 6 =PPVCORE_S0_CPU

U1000
LYNNFIELD
LGA1156-SKT
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OMIT

CPU CORE SUPPLY

A23	VCC_0	VTT_0	AA33
A24	VCC_1	VTT_1	AA34
A26	VCC_2	VTT_2	AA35
A27	VCC_3	VTT_3	AA36
A33	VCC_4	VTT_4	AA37
A35	VCC_5	VTT_5	AA38
A36	VCC_6	VTT_6	AB7
B23	VCC_7	VTT_7	AC33
B25	VCC_8	VTT_8	AC34
B26	VCC_9	VTT_9	AC35
B28	VCC_10	VTT_10	AC36
B29	VCC_11	VTT_11	AC37
B31	VCC_12	VTT_12	AC38
B32	VCC_13	VTT_13	AC39
B34	VCC_14	VTT_14	AC40
B35	VCC_15	VTT_15	AC5
B37	VCC_16	VTT_16	AC8
B38	VCC_17	VTT_17	AD33
C23	VCC_18	VTT_18	AD34
C24	VCC_19	VTT_19	AD35
C25	VCC_20	VTT_20	AD36
C27	VCC_21	VTT_21	AD37
C28	VCC_22	VTT_22	AD38
C30	VCC_23	VTT_23	AD39
C31	VCC_24	VTT_24	AD40
C33	VCC_25	VTT_25	AE33
C34	VCC_26	VTT_26	AE34
C36	VCC_27	VTT_27	AE39
C37	VCC_28	VTT_28	AE40
C39	VCC_29	VTT_29	AE8
D23	VCC_30	VTT_30	AF33
D24	VCC_31	VTT_31	AG33
D26	VCC_32	VTT_32	AJ17
D27	VCC_33	VTT_33	AJ19
D29	VCC_34	VTT_34	AJ21
D30	VCC_35	VTT_35	AJ23
D32	VCC_36	VTT_36	AJ25
D33	VCC_37	VTT_37	AJ27
D35	VCC_38	VTT_38	AJ29
D36	VCC_39	VTT_39	AJ31
D38	VCC_40	VTT_40	AJ32
D39	VCC_41	VTT_41	AK19
E22	VCC_42	VTT_42	AK20
E23	VCC_43	VTT_43	AK21
E25	VCC_44	VTT_44	AL20
E26	VCC_45	VTT_45	AL21
E28	VCC_46	VTT_46	L10
E29	VCC_47	VTT_47	M10
E31	VCC_48	VTT_48	M11
E32	VCC_49	VTT_49	M9
E34	VCC_50	VTT_50	N7
E35	VCC_51	VTT_51	P6
E37	VCC_52	VTT_52	P7
E38	VCC_53	VTT_53	P8
E40	VCC_54	VTT_54	T2
F21	VCC_55	VTT_55	T6
F22	VCC_56	VTT_56	T7
F24	VCC_57	VTT_57	T8
F25	VCC_58	VTT_58	V2
F27	VCC_59	VTT_59	V33
F28	VCC_60	VTT_60	V34
F30	VCC_61	VTT_61	V35
F31	VCC_62	VTT_62	V36
F33	VCC_63	VTT_63	V37
F34	VCC_64	VTT_64	V38
F36	VCC_65	VTT_65	V39
F37	VCC_66	VTT_66	V40
F39	VCC_67	VTT_67	V6
F40	VCC_68	VTT_68	V7
G20	VCC_69	VTT_69	V8
G21	VCC_70	VTT_70	W1
G23	VCC_71	VTT_71	W6
G24	VCC_72	VTT_72	Y33
G26	VCC_73	VTT_73	Y34
G27	VCC_74	VTT_74	Y35
G29	VCC_75	VTT_75	Y36
G30	VCC_76	VTT_76	Y37
G32	VCC_77	VTT_77	Y38
G33	VCC_78		
G35	VCC_79		
G36	VCC_80		
G38	VCC_81		
G39	VCC_82		
H19	VCC_83		
H20	VCC_84		
H22	VCC_85		
H23	VCC_86		
H25	VCC_87		
H26	VCC_88		
H28	VCC_89		
H29	VCC_90		
H31	VCC_91		
H32	VCC_92		
H34	VCC_93		
H35	VCC_94		
H37	VCC_95		
H38	VCC_96		
H40	VCC_97		
J18	VCC_98		
J19	VCC_99		

1.1V RAIL POWER

=PPVTT_S0_CPU 6 11 16 46 64
(Controlled by VTT_SELECT pin)

17 6 =PPVAXG_S0_CPU
THIS SUPPLY IS NEEDED ONLY FOR SYSTEM WITH DALE IG

U1000
LYNNFIELD
LGA1156-SKT
(7 OF 10)
OMIT

GRAPHICS

A14	VAXG_0	
A15	VAXG_1	
A17	VAXG_2	
A18	VAXG_3	
B14	VAXG_4	
B15	VAXG_5	
B17	VAXG_6	
B18	VAXG_7	
C14	VAXG_8	
C15	VAXG_9	
C17	VAXG_10	
C18	VAXG_11	
C20	VAXG_12	
C21	VAXG_13	
D14	VAXG_14	
D15	VAXG_15	
D17	VAXG_16	
D18	VAXG_17	
D20	VAXG_18	
D21	VAXG_19	
E14	VAXG_20	
E15	VAXG_21	
E17	VAXG_22	
E18	VAXG_23	
E20	VAXG_24	
F14	VAXG_25	
F15	VAXG_26	
F17	VAXG_27	
F18	VAXG_28	
F19	VAXG_29	
G14	VAXG_30	
G15	VAXG_31	
G17	VAXG_32	
G18	VAXG_33	
H14	VAXG_34	
H15	VAXG_35	
H17	VAXG_36	
J14	VAXG_37	
J15	VAXG_38	
J16	VAXG_39	
K14	VAXG_40	
K15	VAXG_41	
K16	VAXG_42	
L14	VAXG_43	
L15	VAXG_44	
L16	VAXG_45	
M14	VAXG_46	
M15	VAXG_47	
M16	VAXG_48	

SENSE LINES

VSSAXG_SENSE	B13	TP_GFX_VSENSE_N 8
VAXG_SENSE	A13	TP_GFX_VSENSE_P 8

GRAPHICS VIDS

GFX_VID_0	G10	TP_GFX_VID<0> 8
GFX_VID_1	B12	TP_GFX_VID<1> 8
GFX_VID_2	E12	TP_GFX_VID<2> 8
GFX_VID_3	E11	TP_GFX_VID<3> 8
GFX_VID_4	C12	TP_GFX_VID<4> 8
GFX_VID_5	G11	TP_GFX_VID<5> 8
GFX_VID_6	J11	TP_GFX_VID<6> 8
GFX_VR_EN	F12	TP_GFX_VR_EN
GFX_DPRSLPVR	J10	TP_GFX_DPRSLPVR
GFX_IMON	F6	

POWER

=PP1V5_CPU_MEM 6 11 16 29

DDR3-1.5V RAILS

VDDQ_0	AJ11	
VDDQ_1	AJ13	
VDDQ_2	AJ15	
VDDQ_3	AT10	
VDDQ_4	AT18	
VDDQ_5	AT21	
VDDQ_6	AU11	
VDDQ_7	AV13	
VDDQ_8	AV16	
VDDQ_9	AV19	
VDDQ_10	AV22	
VDDQ_11	AV25	
VDDQ_12	AV28	
VDDQ_13	AW9	
VDDQ_14	AY11	
VDDQ_15	AY14	
VDDQ_16	AY17	
VDDQ_17	AY23	
VDDQ_18	AY26	

=PP1V8_S0_CPU_PLL 6 16 63

1.8V

VCCPLL_0	AF7	
VCCPLL_1	AF8	
VCCPLL_2	AG8	

CPU VIDS

PSI*	AG38	CPU_PSI_L OUT 16 64 89
VID_0/MSID_0	U40	CPU_VID<0> OUT 16 64 89
VID_1/MSID_1	U39	CPU_VID<1> OUT 16 64 89
VID_2/MSID_2	U38	CPU_VID<2> OUT 16 64 89
VID_3/CSC_0	U37	CPU_VID<3> OUT 16 64 89
VID_4/CSC_1	U36	CPU_VID<4> OUT 16 64 89
VID_5/CSC_2	U35	CPU_VID<5> OUT 16 64 89
VID_6	U34	CPU_VID<6> OUT 16 64 89
VID_7	U33	CPU_VID<7> OUT 16 64 89
VTT_SELECT	AF39	TP_CPU_VTTSELECT

SENSE LINES

ISENSE	T40	VR_CPU_IOUT (CONNECTED TO THE IMON OUT FROM CPU REG) IN 64 88
VCC_SENSE	T35	CPU_VCC_PKG_SENSE_P OUT 49 64 89
VSS_SENSE	T34	CPU_VCC_PKG_SENSE_N OUT 64 89
VTT_SENSE	AE35	CPU_VTTSENSE_P OUT 49 67 89
VSS_SENSE_VTT	AE36	CPU_VTTSENSE_N OUT 67 89

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
CPU POWER

Apple Inc.

DRAWING NUMBER 051-8233
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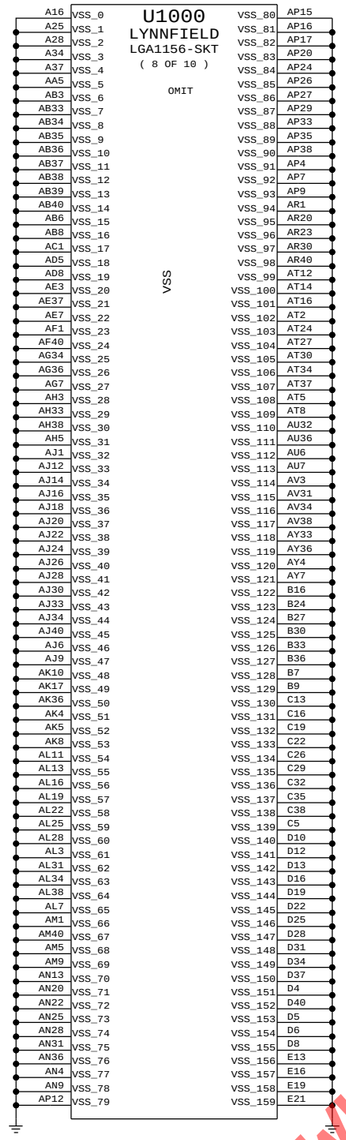
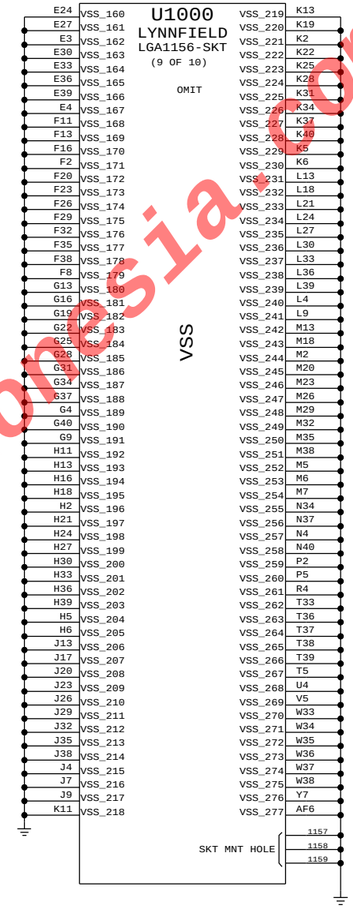
REVISION B.0.0
BRANCH
PAGE 13 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





PAGE TITLE
CPU GROUNDS

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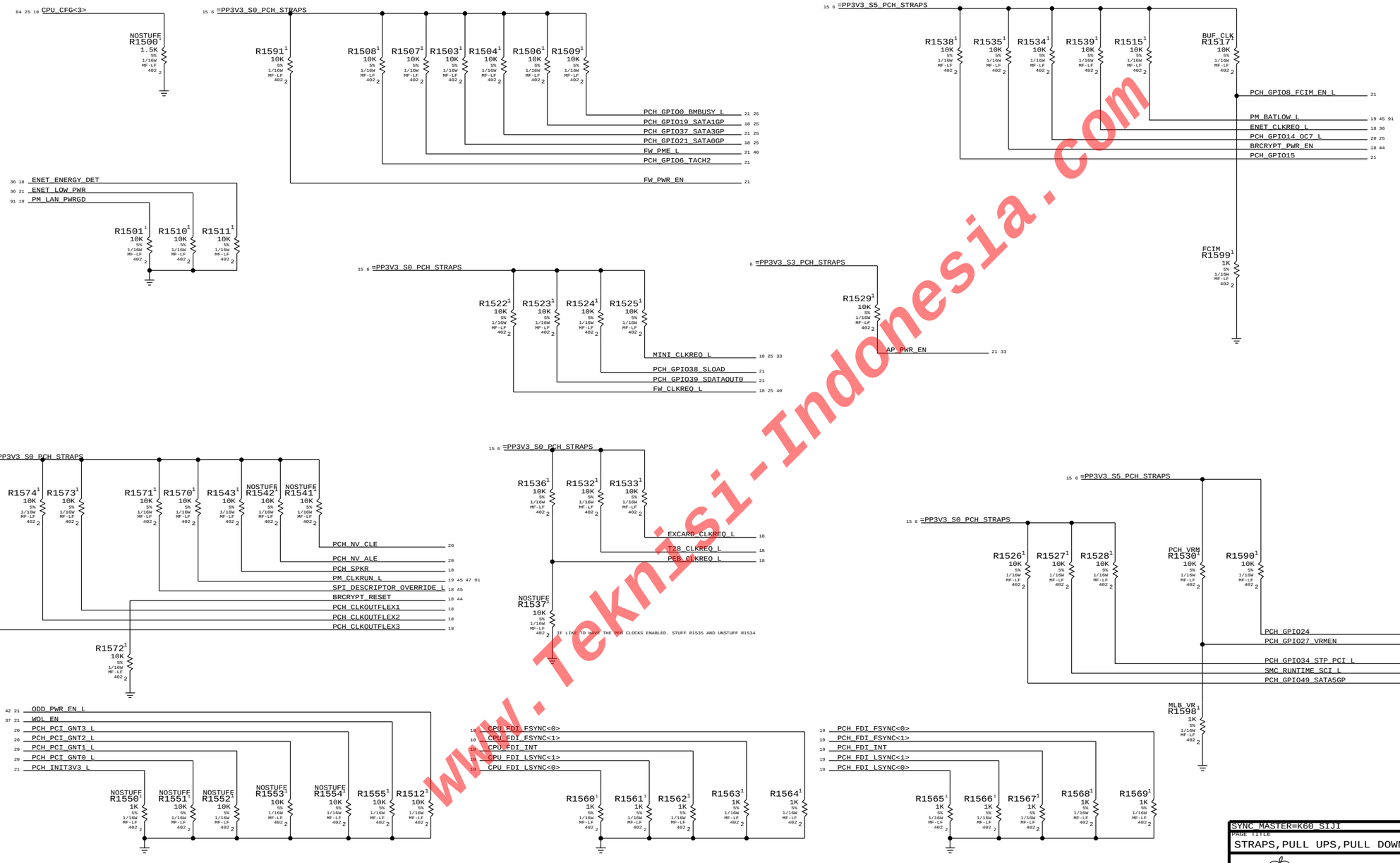
SHEET 1



SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE

STRAPS,PULL UPS,PULL DOWNS FOR PCH AND CPU

Apple Inc.

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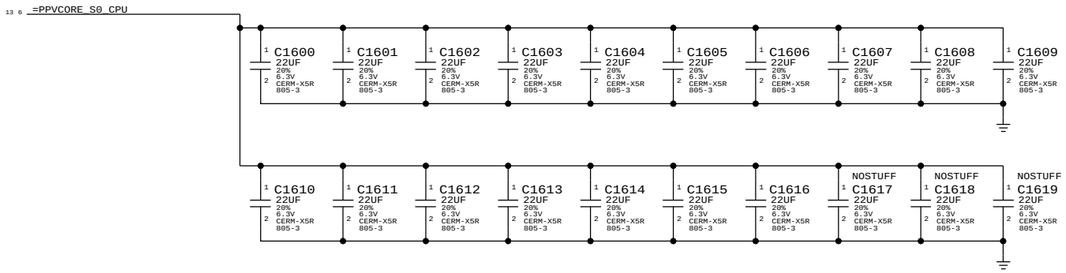
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CPU VCORE DECOUPLING

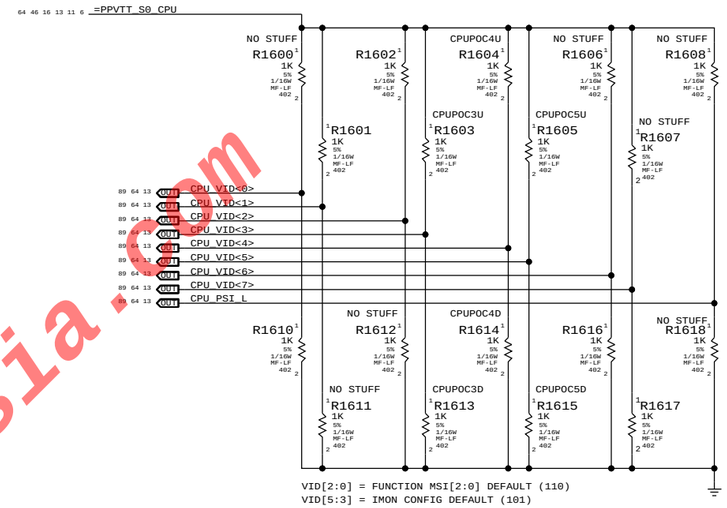
INTEL RECOMMENDATION 17X 22UF 0805



BULK CAPS ON CPU VREG PAGE 74

CPU Power On Configuration (POC) Straps

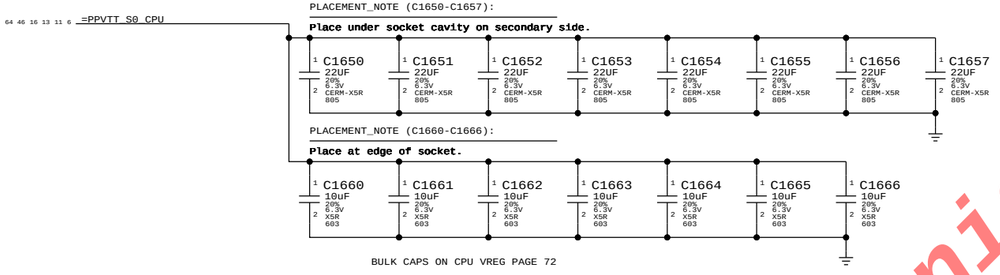
Intel recommends all option straps should be provided in layout



VID[2:0] = FUNCTION MSI[2:0] DEFAULT (110)
VID[5:3] = IMON CONFIG DEFAULT (101)
VID[6] = Reserved (0)
VID[7] = VRD SELECT (0)
PSI# = Reserved (0)

VTT (CPU Uncore) DECOUPLING

8X 22UF 0805, 7X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805



BULK CAPS ON CPU VREG PAGE 72

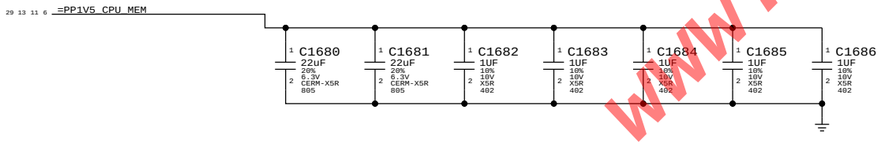
MSI : MARKET SEGMENT IDENTIFICATION
PREVENTS THE PLATFORM BOOTING USING A HIGHER POWERED CPU

BOM GROUP	IMAX @ 900mV	CPU Gain Setting	BOM OPTIONS	Equivalent Gain
CPUPOC_IMAX_DIS		000	CPUPOC3D,CPUPOC4D,CPUPOC5D	
CPUPOC_IMAX_0_40	40A	001	CPUPOC3D,CPUPOC4D,CPUPOC5D	45
CPUPOC_IMAX_40_60	60A	010	CPUPOC3D,CPUPOC4U,CPUPOC5D	30
CPUPOC_IMAX_60_80	80A	011	CPUPOC3D,CPUPOC4U,CPUPOC5U	22.5
CPUPOC_IMAX_80_100	100A	100	CPUPOC3U,CPUPOC4D,CPUPOC5D	18
CPUPOC_IMAX_100_120	120A	101	CPUPOC3U,CPUPOC4D,CPUPOC5U	15
CPUPOC_IMAX_120_140	140A	110	CPUPOC3U,CPUPOC4U,CPUPOC5D	12.857
CPUPOC_IMAX_140_180	180A	111	CPUPOC3U,CPUPOC4U,CPUPOC5U	10

NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONs directly.
Instead call out appropriate BOM GROUP defined in tables above.

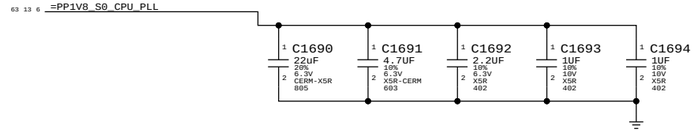
Memory (CPU VCCDDR) DECOUPLING

2x 22uF 0805, 5x 1uF 0402



PLL (CPU VCCSFR) DECOUPLING

1x 22uF 0805, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402



SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
CPU NON-GFX DECOUPLING

Apple Inc.

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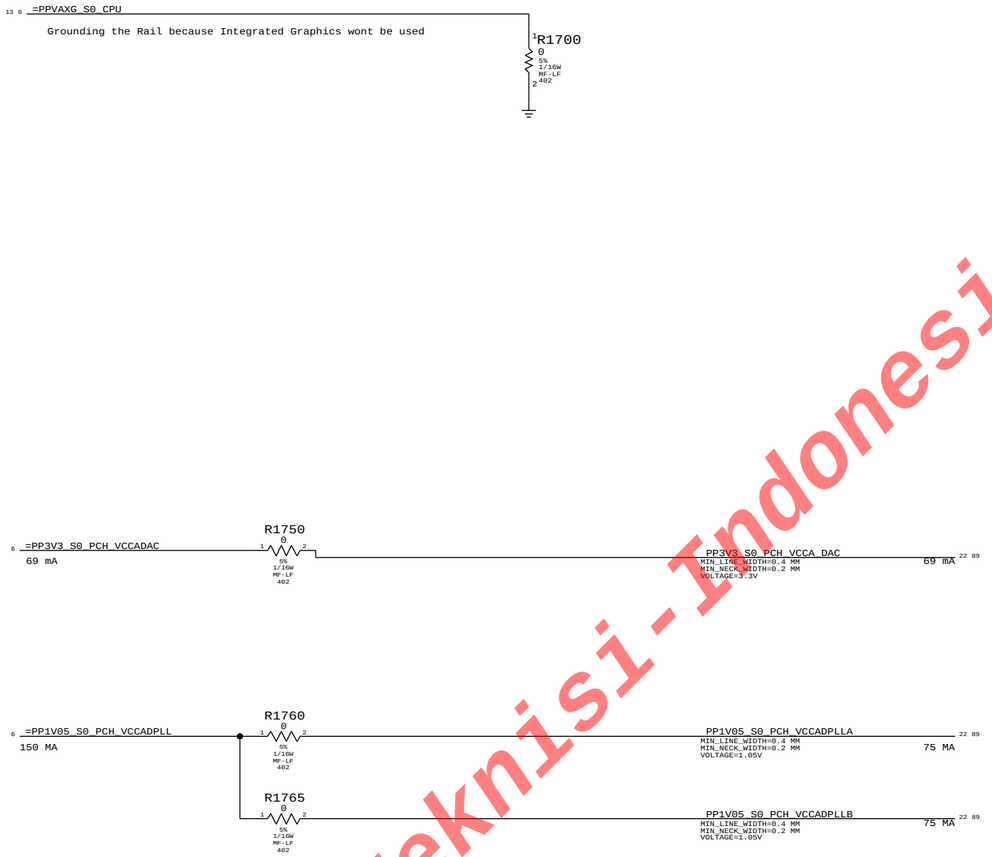
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
CPU/PCH GFX DECOUPLING

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
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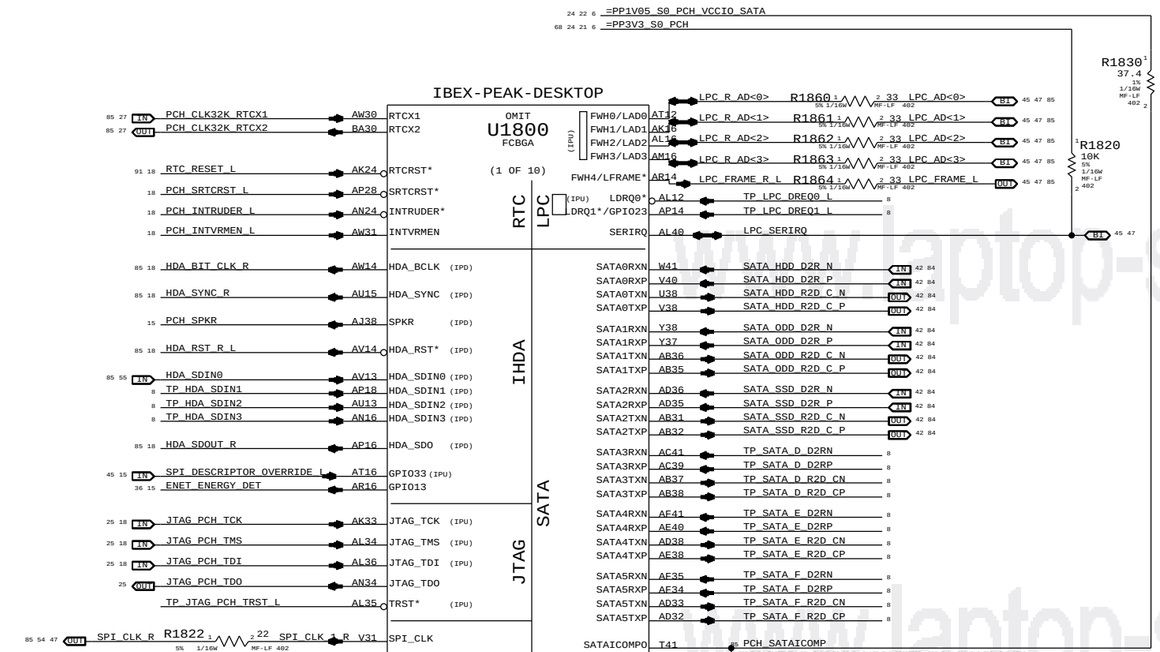
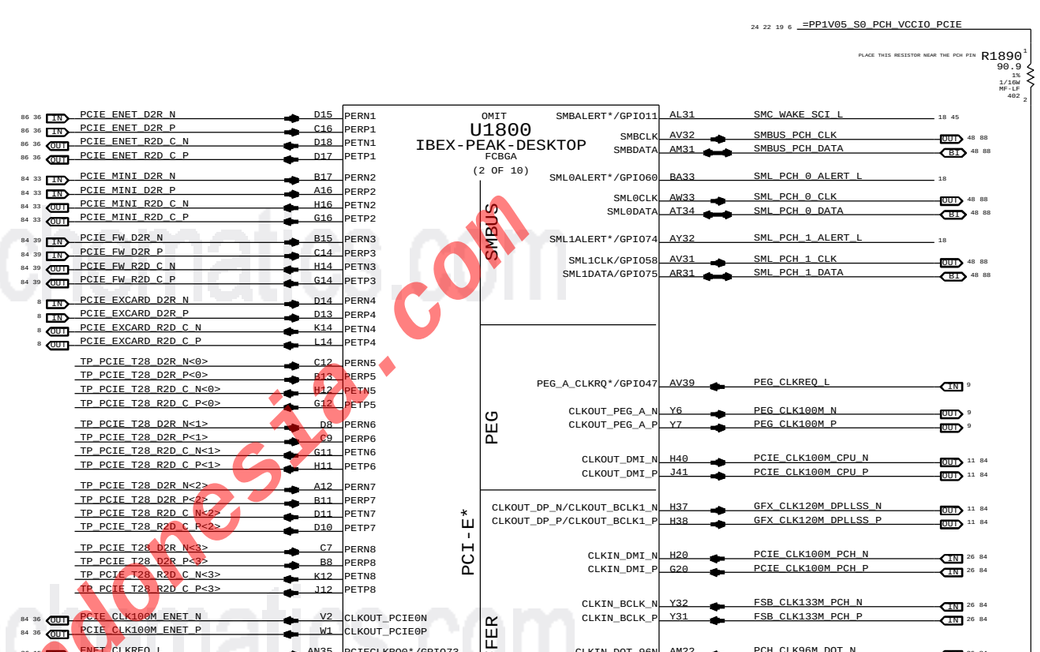
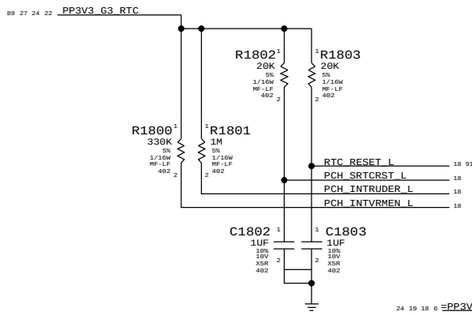
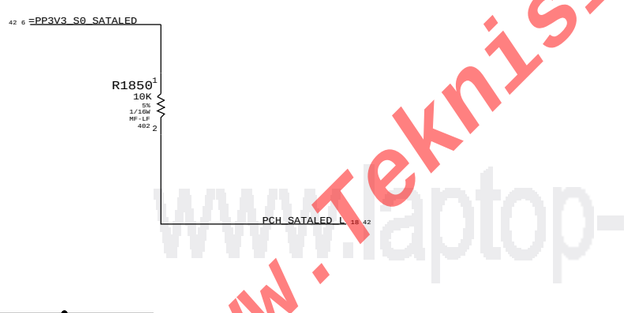
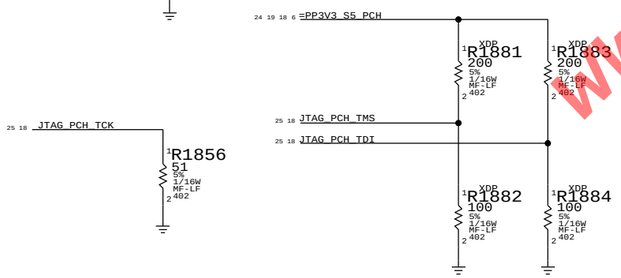
PAGE 17 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

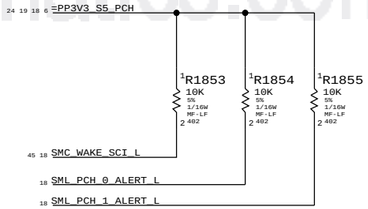












SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI

Apple Inc.

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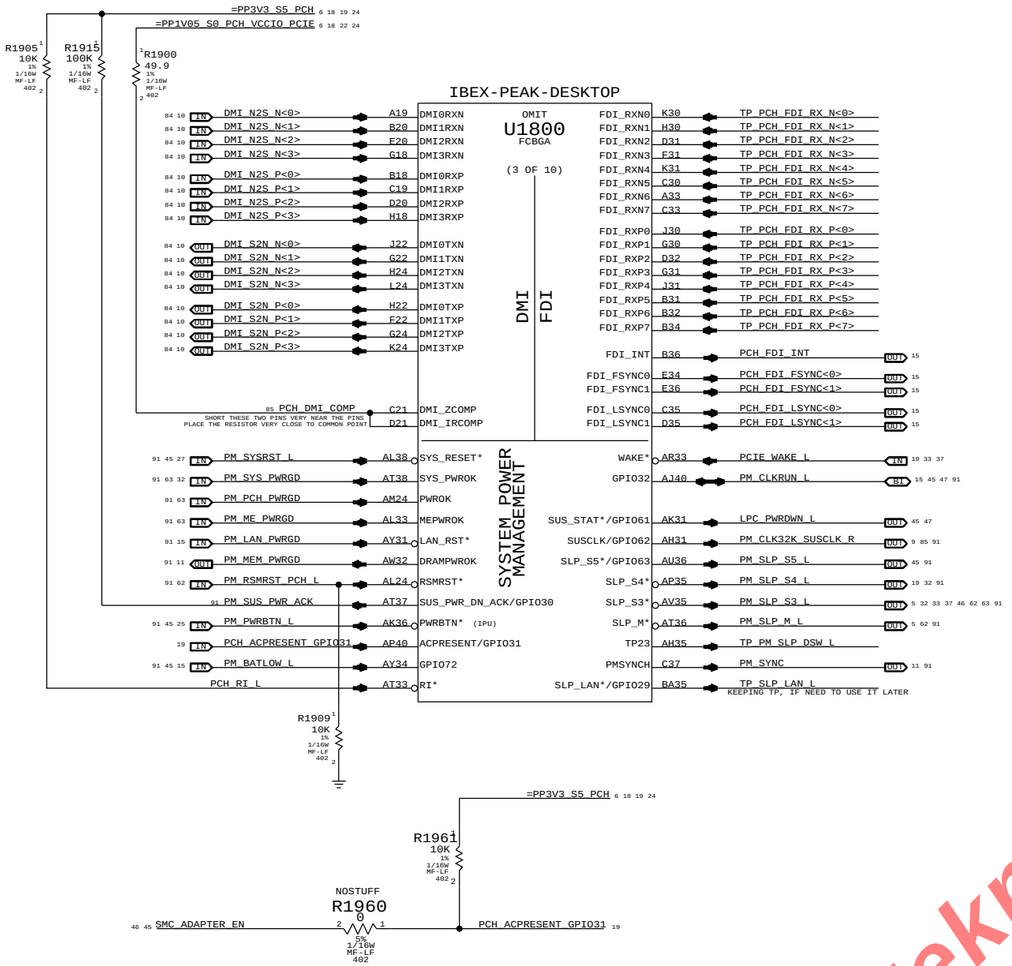
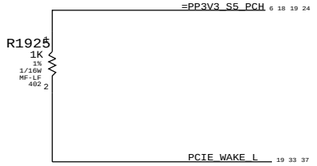
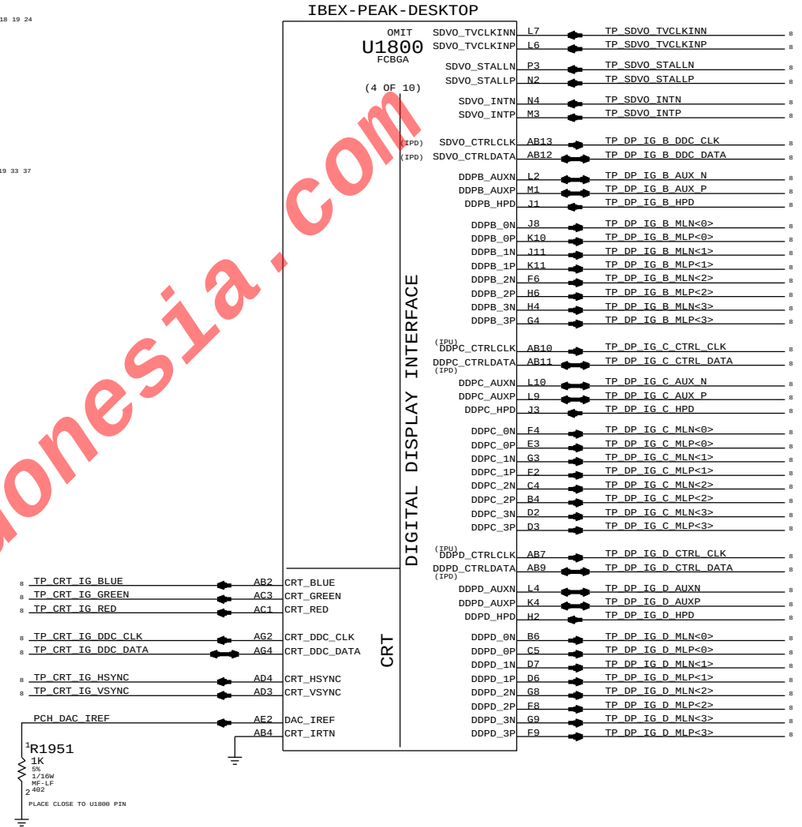
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>







PAGE TITLE
PCH DMI/FDI/GRAPHICS

Apple Inc.

DRAWING NUMBER 051-8233
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SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

IBEX-PEAK-DESKTOP

QMIT
U1800
FCBGA
(5 OF 10)

PCI

TP_PCI_AD<0>	AT9	AD0	
TP_PCI_AD<1>	AP11	AD1	
TP_PCI_AD<2>	AU6	AD2	
TP_PCI_AD<3>	AY10	AD3	
TP_PCI_AD<4>	AP9	AD4	
TP_PCI_AD<5>	AV8	AD5	
TP_PCI_AD<6>	AR9	AD6	
TP_PCI_AD<7>	AV7	AD7	
TP_PCI_AD<8>	AW9	AD8	
TP_PCI_AD<9>	AR3	AD9	
TP_PCI_AD<10>	AW7	AD10	
TP_PCI_AD<11>	AR8	AD11	
TP_PCI_AD<12>	AU3	AD12	
TP_PCI_AD<13>	AP2	AD13	
TP_PCI_AD<14>	AU1	AD14	
TP_PCI_AD<15>	AN3	AD15	
TP_PCI_AD<16>	AM2	AD16	
TP_PCI_AD<17>	AM11	AD17	
TP_PCI_AD<18>	AM4	AD18	
TP_PCI_AD<19>	AY8	AD19	
TP_PCI_AD<20>	AL10	AD20	
TP_PCI_AD<21>	AT5	AD21	
TP_PCI_AD<22>	AL2	AD22	
TP_PCI_AD<23>	AT2	AD23	
TP_PCI_AD<24>	AL4	AD24	
TP_PCI_AD<25>	AV10	AD25	
TP_PCI_AD<26>	AL9	AD26	
TP_PCI_AD<27>	AN7	AD27	
TP_PCI_AD<28>	AK7	AD28	
TP_PCI_AD<29>	AN6	AD29	
TP_PCI_AD<30>	AH12	AD30	
TP_PCI_AD<31>	AN11	AD31	
TP_PCI_C_BE_L<0>	AV3	C/BE0*	
TP_PCI_C_BE_L<1>	AY6	C/BE1*	
TP_PCI_C_BE_L<2>	AP5	C/BE2*	
TP_PCI_C_BE_L<3>	AW10	C/BE3*	
PCI_INTA_L	AT8	PIRQA*	
PCI_INTB_L	AR4	PIRQB*	
PCI_INTC_L	AT11	PIRQC*	
PCI_INTD_L	BA5	PIRQD*	
PCI_REQ0_L	AP4	REQ0*	
PCI_REQ1_L	AW5	REQ1*/GPIO50	
PCI_REQ2_L	AY4	REQ2*/GPIO52	
PCI_REQ3_L	AH8	REQ3*/GPIO54	
PCH_PCI_GNT0_L	AK11	GNT0* (IPU)	
PCH_PCI_GNT1_L	AK6	GNT1*/GPIO51	
PCH_PCI_GNT2_L	BA9	GNT2*/GPIO53	
PCH_PCI_GNT3_L	AM3	GNT3*/GPIO55	
PCI_INTE_L	AU8	PIRQE*/GPIO2	
AUD_IP_PERIPHERAL_DET	AH7	PIRQF*/GPIO3	
PCI_INTG_L	AP12	PIRQG*/GPIO4	
AUD_I2C_INT_L	AW4	PIRQH*/GPIO5	
TP_PCI_RESET_L	AH10	PCIRST*	
PCI_SERR_L	AV6	SERR*	
PCI_PERR_L	AT4	PERR*	
PCI_IRDY_L	AP7	IRDY*	
TP_PCI_PAR	AP6	PAR	
PCI_DEVSEL_L	AT6	DEVSEL*	
PCI_FRAME_L	AL7	FRAME*	
PCI_PLOCK_L	AK12	PLOCK*	
PCI_STOP_L	AN8	STOP*	
PCI_TRDY_L	AL6	TRDY*	
TP_PCI_PME_L	AH11	PME* (IPU)	
PLT_RESET_L	AV34	PLTRST*	
LPC_CLK33M_SMC_R	AF6	CLKOUT_PCI0	
LPC_CLK33M_LPCPLUS_R	AD7	CLKOUT_PCI1	
TP_PCI_CLK33M_OUT2	AF9	CLKOUT_PCI2	
TP_PCI_CLK33M_OUT3	AD9	CLKOUT_PCI3	
PCH_CLK33M_PCIOUT	AD12	CLKOUT_PCI4	

=PP3V3_S0_PCH_GPIO

R2010 10K 5% 1/16W MF-LF 402
R2011 10K 5% 1/16W MF-LF 402
R2012 10K 5% 1/16W MF-LF 402
R2013 10K 5% 1/16W MF-LF 402
R2015 10K 5% 1/16W MF-LF 402
R2016 10K 5% 1/16W MF-LF 402
R2017 10K 5% 1/16W MF-LF 402
R2018 10K 5% 1/16W MF-LF 402
R2030 10K 5% 1/16W MF-LF 402
R2031 10K 5% 1/16W MF-LF 402
R2020 10K 5% 1/16W MF-LF 402
R2021 10K 5% 1/16W MF-LF 402
R2022 10K 5% 1/16W MF-LF 402
R2023 10K 5% 1/16W MF-LF 402
R2024 10K 5% 1/16W MF-LF 402
R2027 10K 5% 1/16W MF-LF 402
R2025 10K 5% 1/16W MF-LF 402
R2026 10K 5% 1/16W MF-LF 402

NVRAM

NV_CE0*	H36	TP_NV_CE_L<0>
NV_CE1*	H35	TP_NV_CE_L<1>
NV_CE2*	P32	TP_NV_CE_L<2>
NV_CE3*	E41	TP_NV_CE_L<3>
NV_DQS0	P36	TP_NV_DQS<0>
NV_DQS1	F40	TP_NV_DQS<1>
NV_DQ0/NV_IO0	T33	TP_NV_DQ<0>
NV_DQ1/NV_IO1	P35	TP_NV_DQ<1>
NV_DQ2/NV_IO2	T31	TP_NV_DQ<2>
NV_DQ3/NV_IO3	P33	TP_NV_DQ<3>
NV_DQ4/NV_IO4	M35	TP_NV_DQ<4>
NV_DQ5/NV_IO5	L33	TP_NV_DQ<5>
NV_DQ6/NV_IO6	M36	TP_NV_DQ<6>
NV_DQ7/NV_IO7	M34	TP_NV_DQ<7>
NV_DQ8/NV_IO8	M30	TP_NV_DQ<8>
NV_DQ9/NV_IO9	F36	TP_NV_DQ<9>
NV_DQ10/NV_IO10	H33	TP_NV_DQ<10>
NV_DQ11/NV_IO11	F37	TP_NV_DQ<11>
NV_DQ12/NV_IO12	E39	TP_NV_DQ<12>
NV_DQ13/NV_IO13	G33	TP_NV_DQ<13>
NV_DQ14/NV_IO14	D40	TP_NV_DQ<14>
NV_DQ15/NV_IO15	F33	TP_NV_DQ<15>
(IPD) NV_ALE	J34	PCH_NV_ALE
(IPD) NV_CLE	L35	PCH_NV_CLE
NV_RCOMP	L36	TP_NV_RCOMP
(IPU) NV_RB*	M32	TP_NV_RB_L
NV_WR0_RE*	J36	TP_NV_WR_RE_L<0>
NV_WR1_RE*	J35	TP_NV_WR_RE_L<1>
NV_WE_CK0*	M31	TP_NV_WE_CK_L<0>
NV_WE_CK1*	F38	TP_NV_WE_CK_L<1>

USB

NOTE: Internal pull-downs on all USB pins

EHCI1 (OPD)

USBP0N	AW25	USB_HUB1_UP_N	USB HUB 1
USBP0P	AY25	USB_HUB1_UP_P	
USBP1N	BA23	TP_USB_1N	Unused
USBP1P	AY24	TP_USB_1P	
USBP2N	AW23	USB_BRCRYPT_N	Blu-ray transcript
USBP2P	AY22	USB_BRCRYPT_P	
USBP3N	AR22	TP_USB_3N	Unused
USBP3P	AP22	TP_USB_3P	
USBP4N	AV21	USB_WM_N	WM
USBP4P	AV22	USB_WM_P	
USBP5N	AY20	TP_USB_5N	Unused
USBP5P	AW21	TP_USB_5P	
USBP6N	AK20	TP_USB_6N	Unused
USBP6P	AL20	TP_USB_6P	
USBP7N	AV20	TP_USB_7N	Unused
USBP7P	AW19	TP_USB_7P	

EHCI2 (OPD)

USBP8N	BA19	USB_HUB2_UP_N	USB HUB 2
USBP8P	AY18	USB_HUB2_UP_P	
USBP9N	AM20	TP_USB_9N	Unused
USBP9P	AN20	TP_USB_9P	
USBP10N	AV17	TP_USB_10N	Unused
USBP10P	AV18	TP_USB_10P	
USBP11N	AR20	TP_USB_11N	Unused
USBP11P	AT20	TP_USB_11P	
USBP12N	AK18	TP_USB_12N	Unused
USBP12P	AL18	TP_USB_12P	
USBP13N	AY17	TP_USB_13N	Unused
USBP13P	BA16	TP_USB_13P	

USBRBIAS* AY15 — PCH_USB_RBIAS (TIE TRACES TOGETHER CLOSE TO PINS)
USBRBIAS AV15

R2070 22.6 1% 1/16W MF-LF 402 — PLACE THE RESISTOR CLOSE TO COMMON POINT

OC0*/GPIO59	AT31	PCH_GPIO59_OC0_L
OC1*/GPIO40	AT30	USB_HUB_SOFT_RESET_L
OC2*/GPIO41	AK28	PCH_GPIO41_OC2_L
OC3*/GPIO42	AP30	PCH_GPIO42_OC3_L
OC4*/GPIO43	AP31	PCH_GPIO43_OC4_L
OC5*/GPIO9	AL28	PCH_GPIO9_OC5_L
OC6*/GPIO10	AL30	PCH_GPIO10_OC6_L
OC7*/GPIO14	AM30	PCH_GPIO14_OC7_L

R2060 10K 5% 1/16W MF-LF 402
R2061 10K 5% 1/16W MF-LF 402
R2062 10K 5% 1/16W MF-LF 402
R2067 10K 5% 1/16W MF-LF 402
R2064 10K 5% 1/16W MF-LF 402
R2065 10K 5% 1/16W MF-LF 402
R2066 10K 5% 1/16W MF-LF 402
=PP3V3_S5_PCH_GPIO

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
PCH PCI/FLASHCACHE/USB

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION B.0.0
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PAGE 20 OF 110
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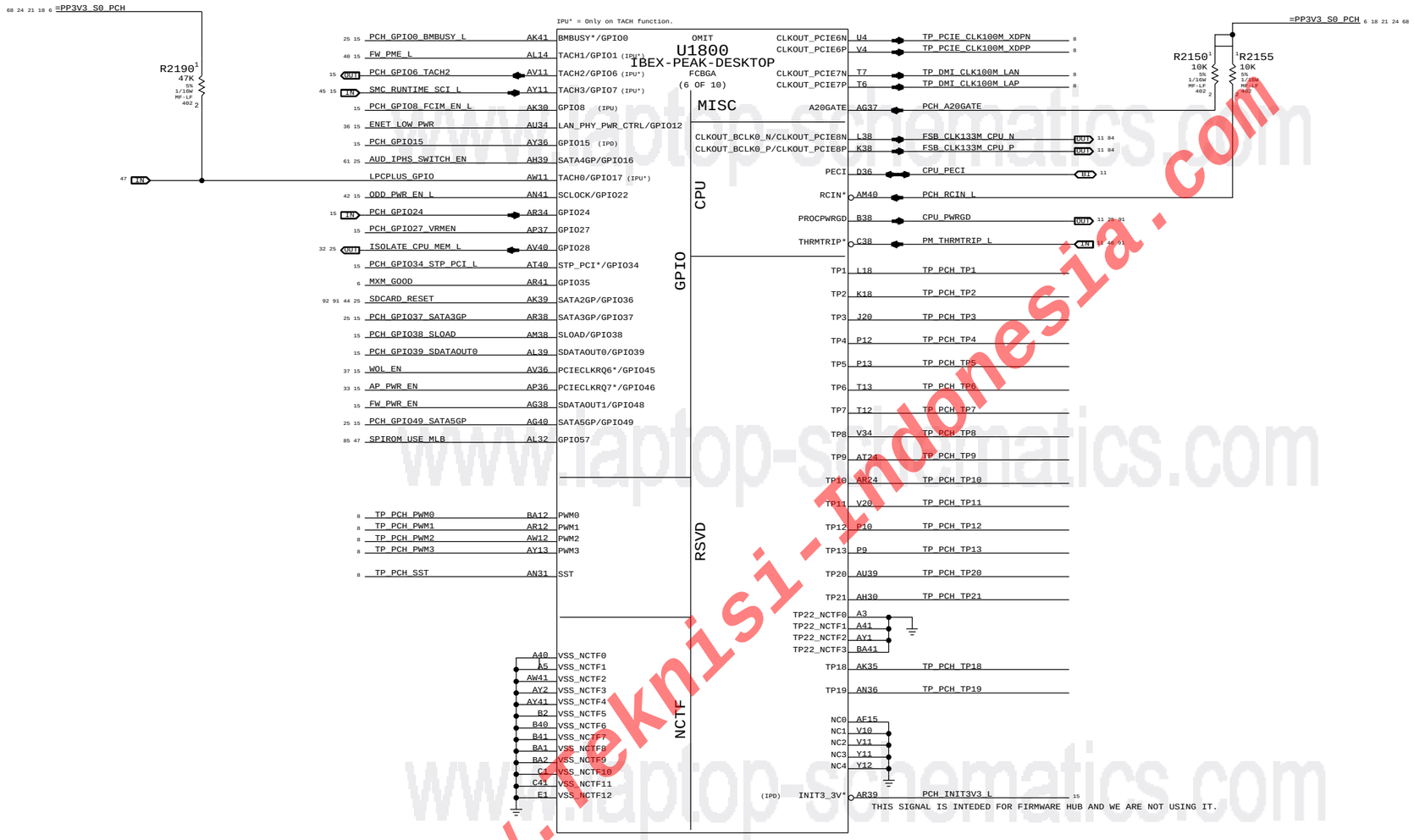

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PAGE TITLE: PCH MISC

Apple Inc.

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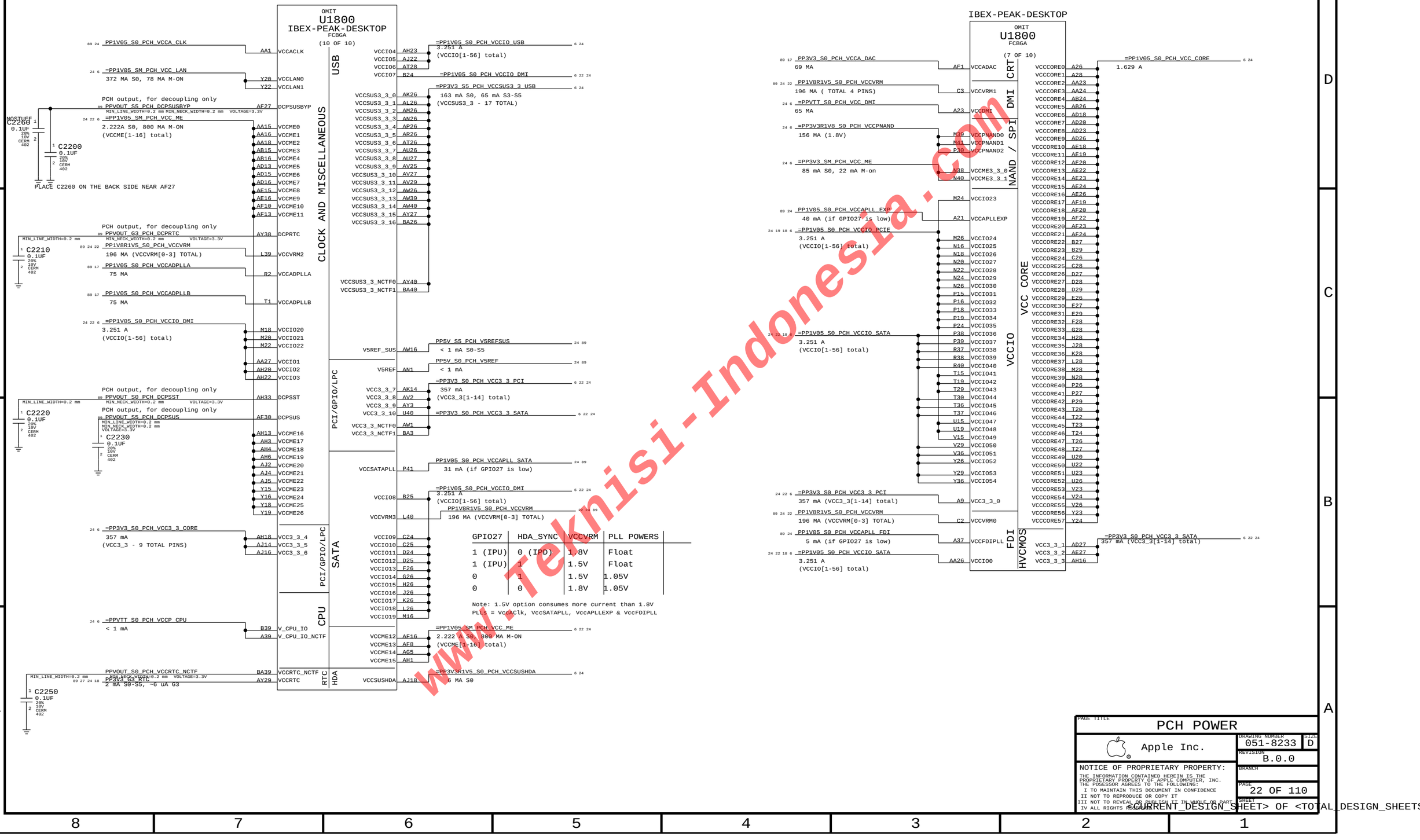

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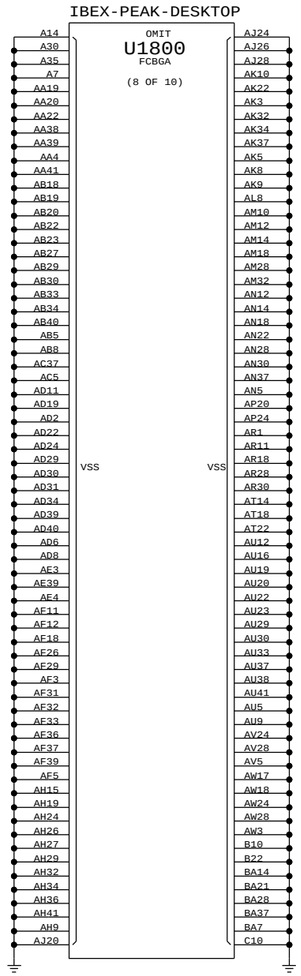

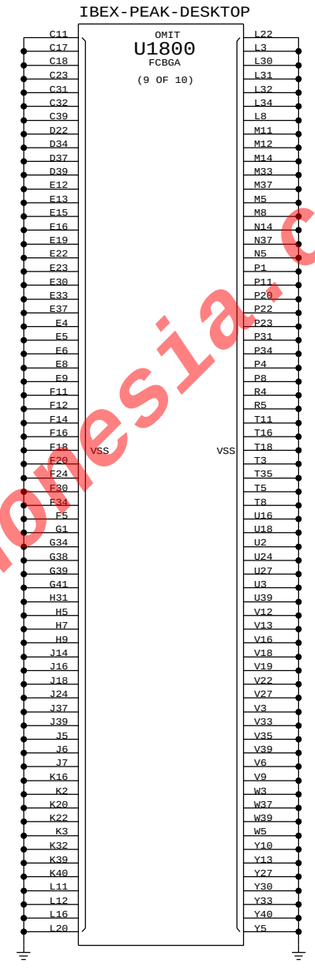

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
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Apple Inc.

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REVISION B.0.0
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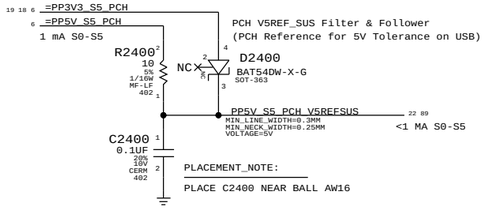
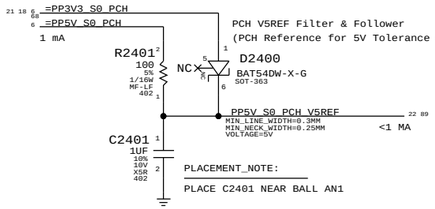
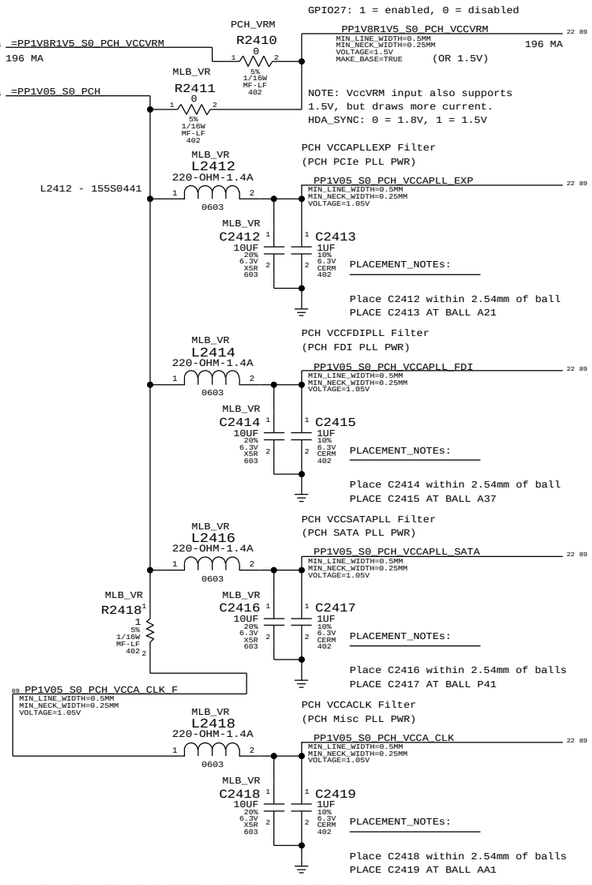
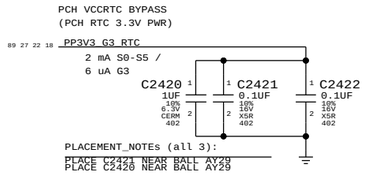
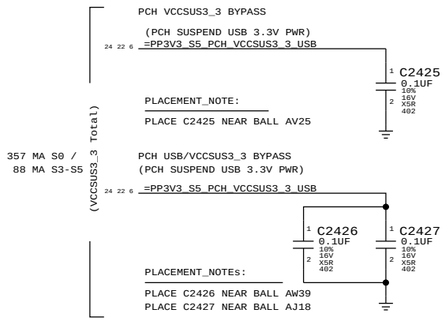


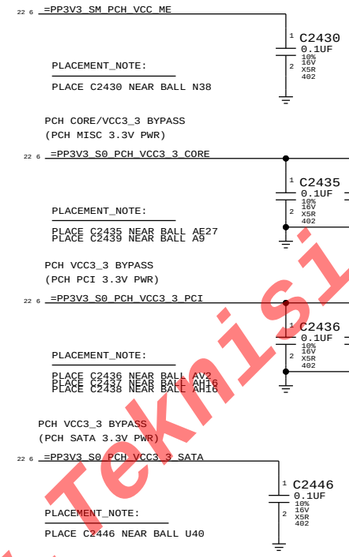


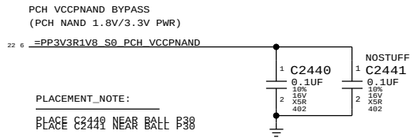


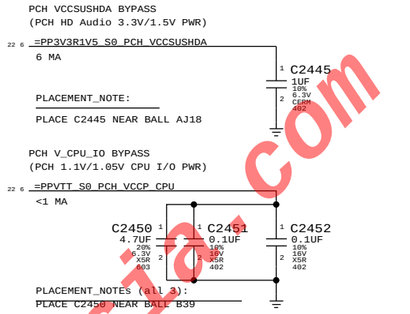
Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

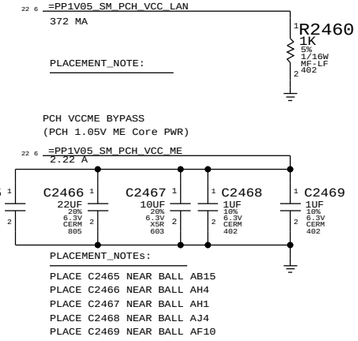


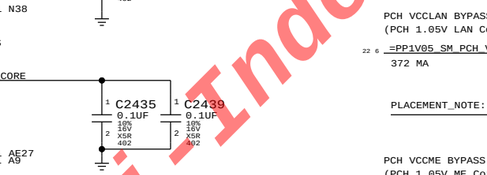


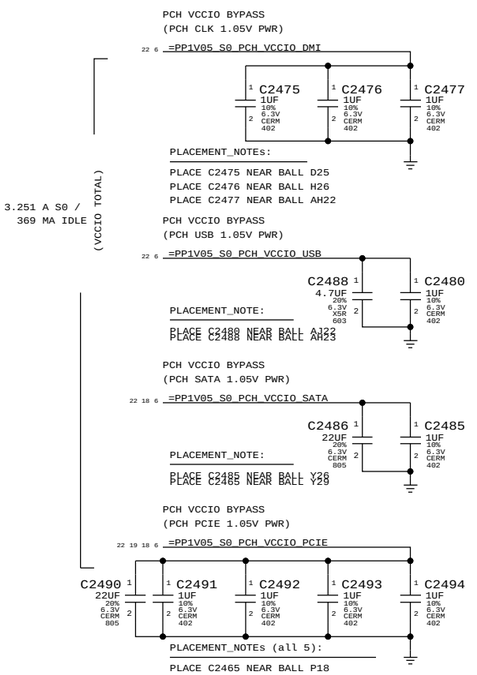












SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE: PCH DECOUPLING

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

REVISION: B.0.0

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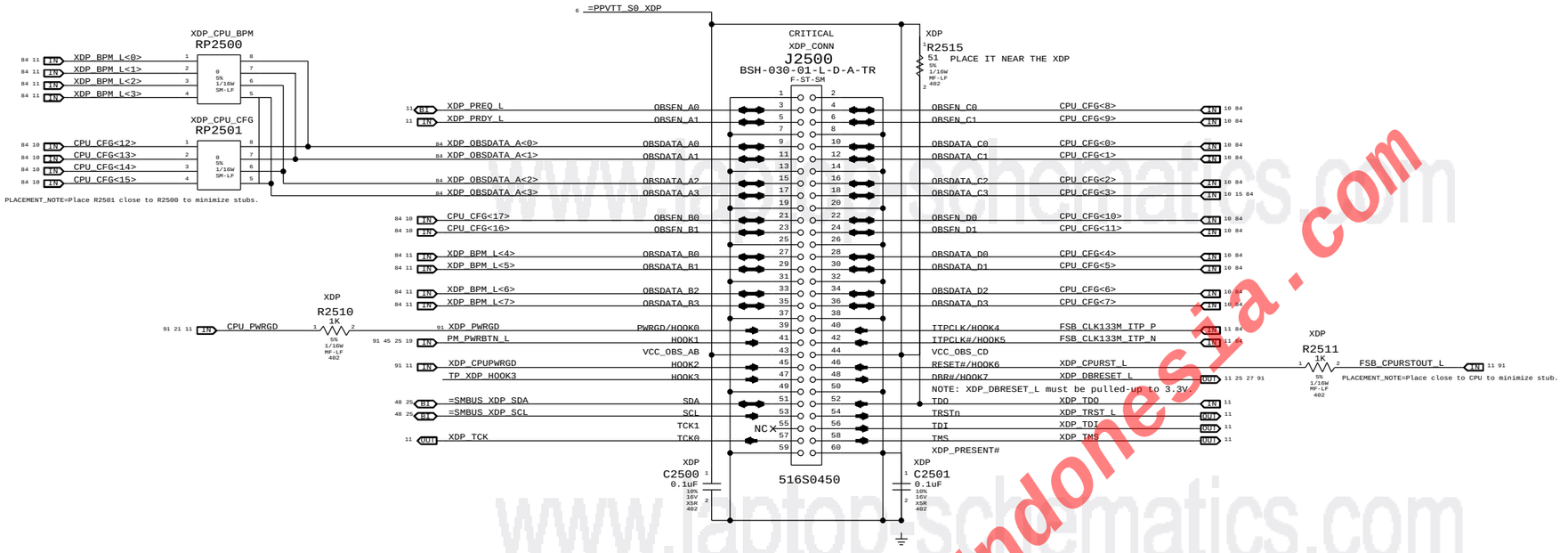
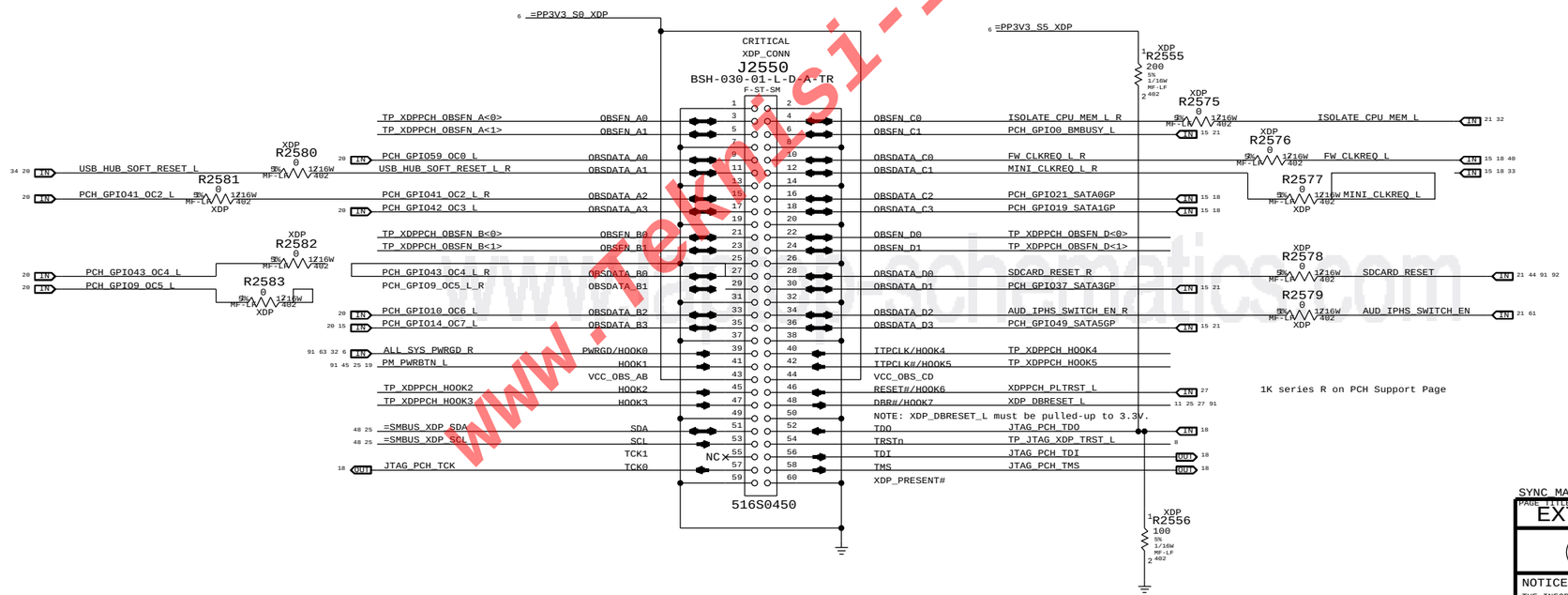
PROCESSOR XDP



PCH XDP



SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE: EXTENDED DEBUG PORT(XDP)

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

REVISION: B.0.0

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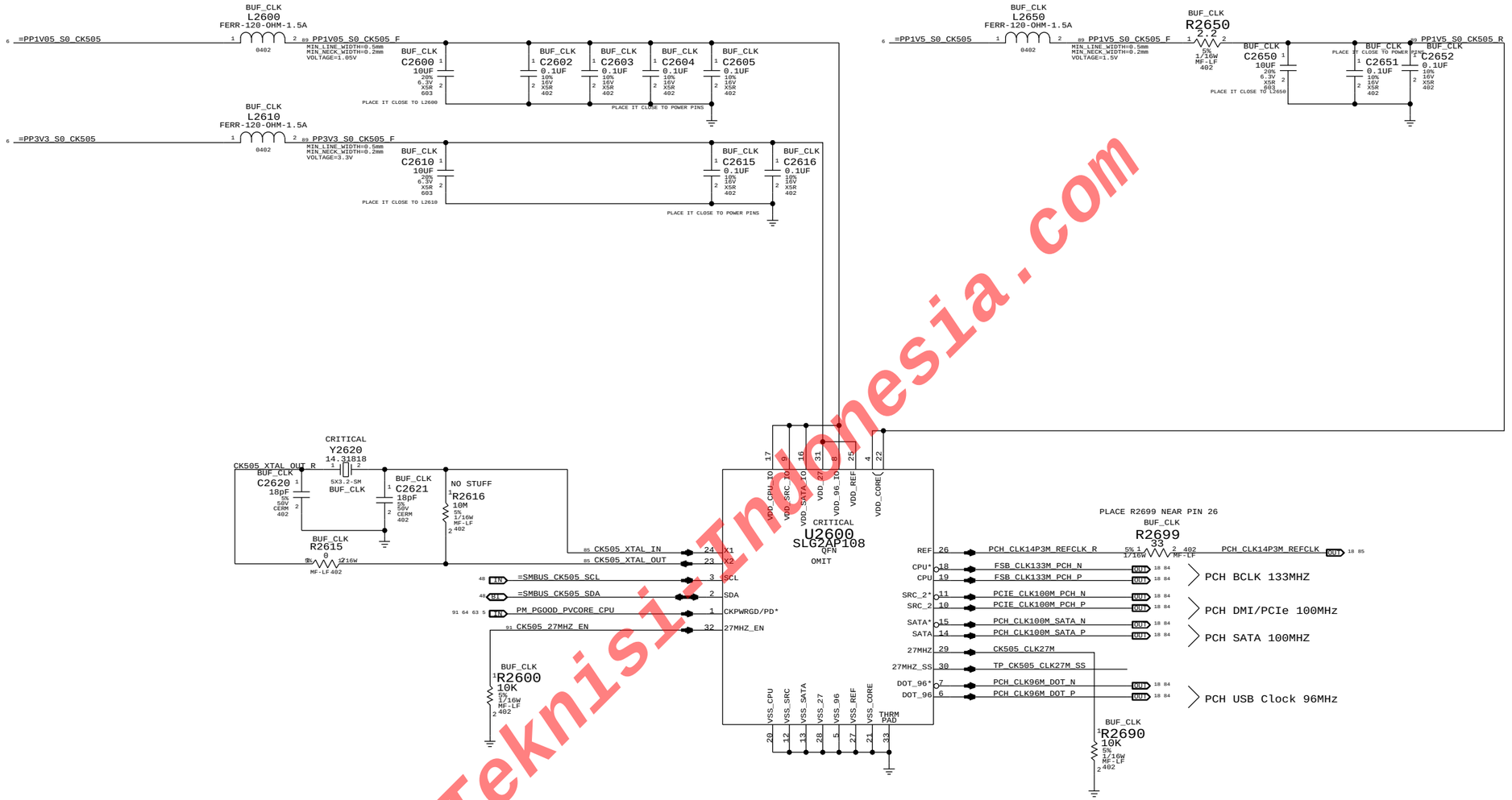

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PAGE TITLE
CLOCK (CK505)

Apple Inc.

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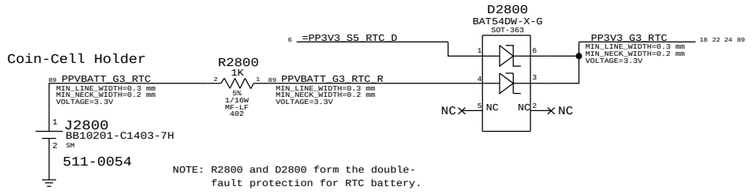
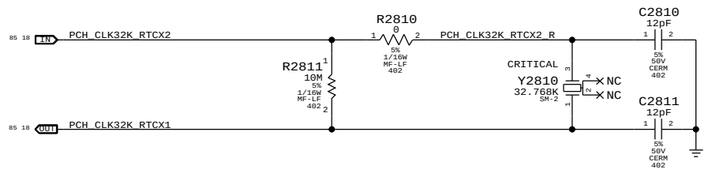
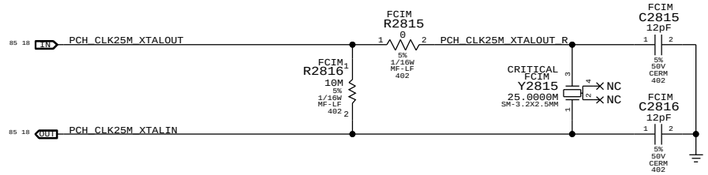
RTC Power Sources



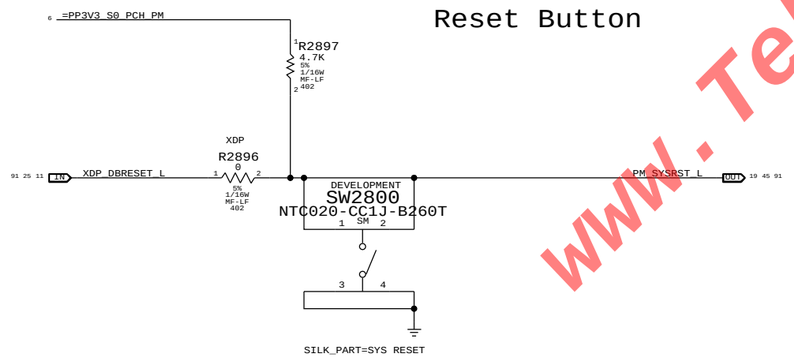
PCH RTC Crystal



PCH 25MHz Crystal

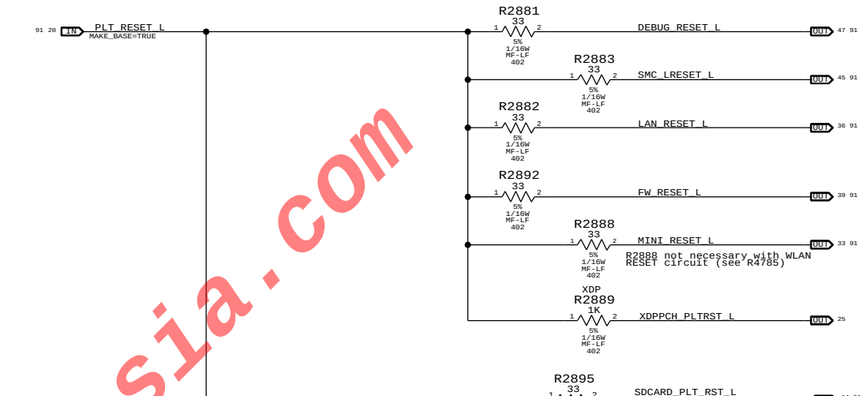


Reset Button



Platform Reset Connections

Unbuffered



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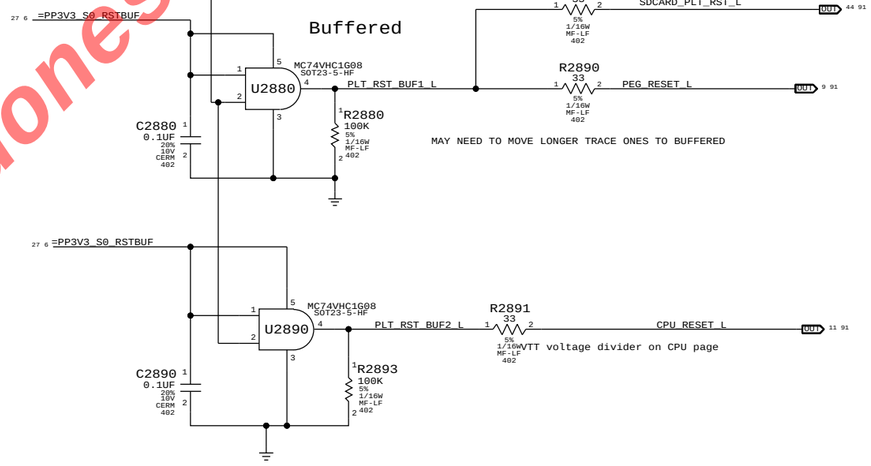

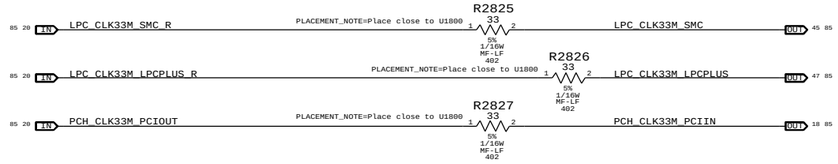

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PAGE TITLE: CHIPSET SUPPORT

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

REVISION: B.0.0

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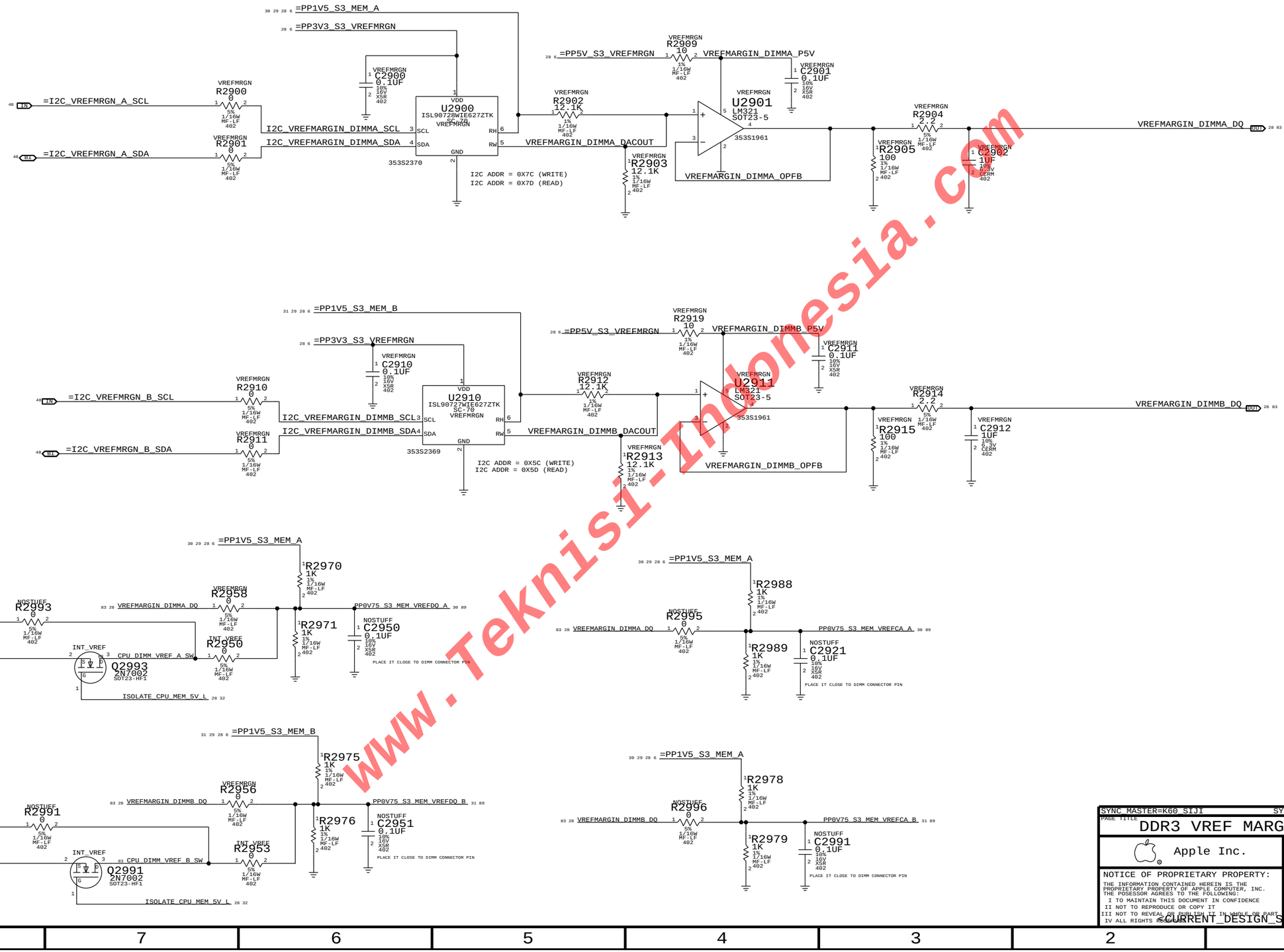

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PAGE TITLE

DDR3 VREF MARGINING

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SHEET

DIMM A (FURTHER FROM CPU) CAPS TO COUPLE CPU 1V5_MEM DIMM B (CLOSER TO CPU)

29 16 13 11 6 =PP1V5_CPU_MEM

C3016 C3017 C3018 C3019 C3010 C3025 C3026 C3027 C3028 C3029 C3020 C3021 C3022 C3023 C3014 C3030 C3031 C3032 C3033

1UF 10% 6.3V CERM 402

EXTRA DECOUPLING CAPS FOR CPU MEM RAIL

29 16 13 11 6 =PP1V5_CPU_MEM

C3041 C3042 C3044 C3046 C3040 C3043 C3045 C3047 C3048 C3049 C3090 C3091 C3092 C3093 C3094

1UF 10% 6.3V CERM 402

29 16 13 11 6 =PP1V5_CPU_MEM

C30A0 C30A1 C30A2 C30A3 C30A4 C30A5 C30A6 C30A7 C30A8 C30A9 C30AA C30AB C30AC C30AD C30AE

1UF 10% 6.3V CERM 402

DECOUPLING CAPS FOR DIMM ON CHANNEL A - AT CONNECTOR

30 28 6 =PP1V5_S3_MEM_A

C3050 10UF 20% 6.3V X5R 603

C3051 10UF 20% 6.3V X5R 603

C3052 C3053 C3054 C3055 C3056 C3057 C3058 C3059 C3060 C3061 C3062 C3063 C3064 C3065 C3066 C3067 C3068 C3069

1UF 10% 6.3V CERM 402

DECOUPLING CAPS FOR DIMM ON CHANNEL B - AT CONNECTOR

31 28 6 =PP1V5_S3_MEM_B

C3070 10UF 20% 6.3V X5R 603

C3071 10UF 20% 6.3V X5R 603

C3072 C3073 C3074 C3075 C3076 C3077 C3078 C3079 C3080 C3081 C3082 C3083 C3084 C3085 C3086 C3087 C3088 C3089

1UF 10% 6.3V CERM 402

SYNC MASTER=K60 SIJI SYNC DATE=07/01/2009

PAGE TITLE: MEMORY CAPS

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

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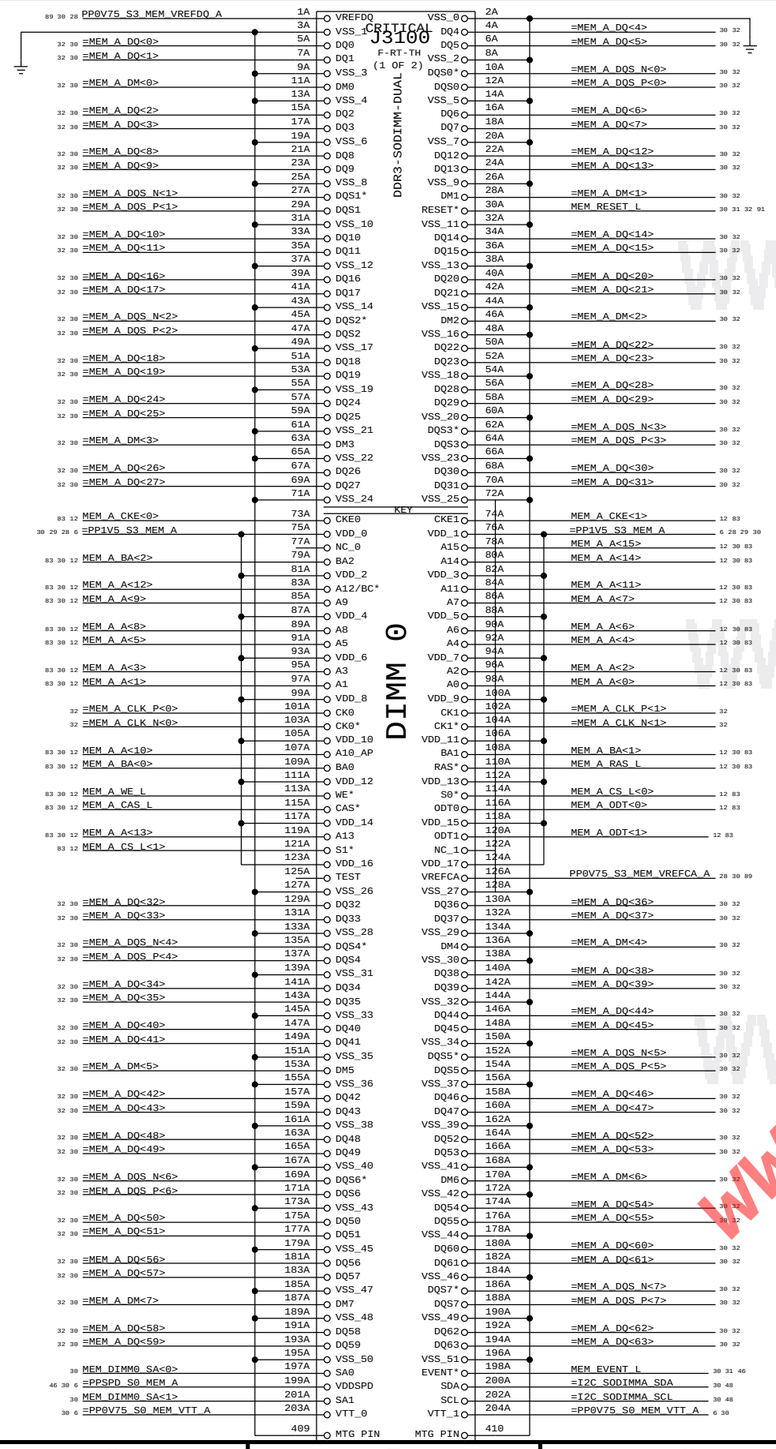
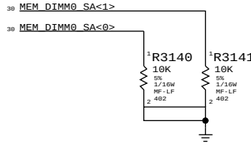
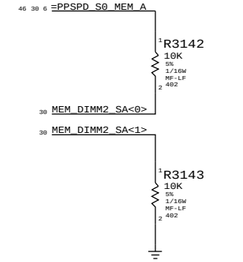
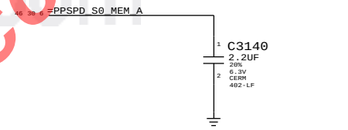


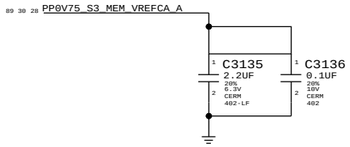
DIMM0 SPD ADDR=0XA0(WR)/0XA1(RD)

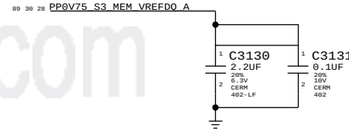


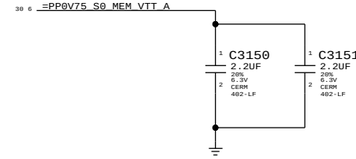
DIMM2 SPD ADDR=0XA2(WR)/0XA3(RD)











Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA
- ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
DDR3 SO-DIMMs 0 & 2

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
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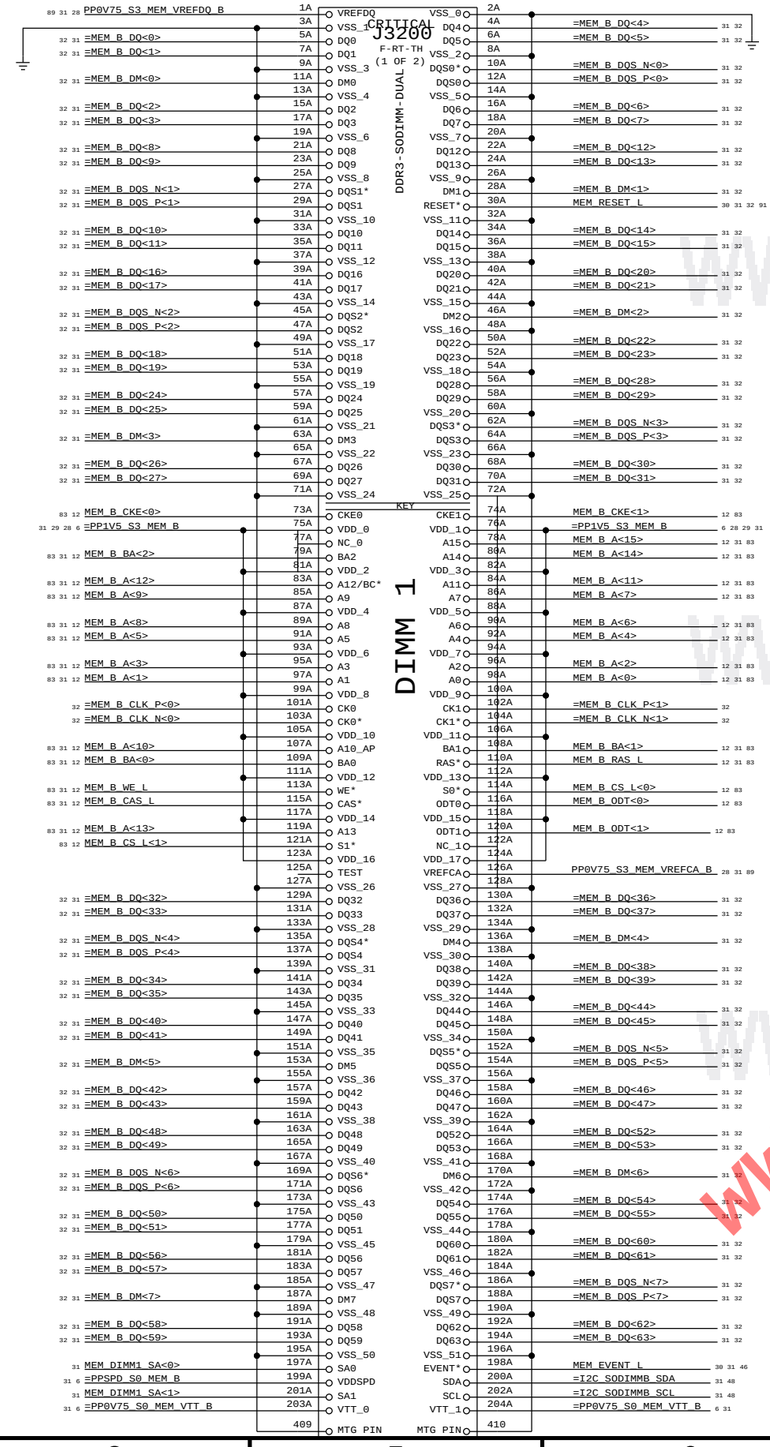

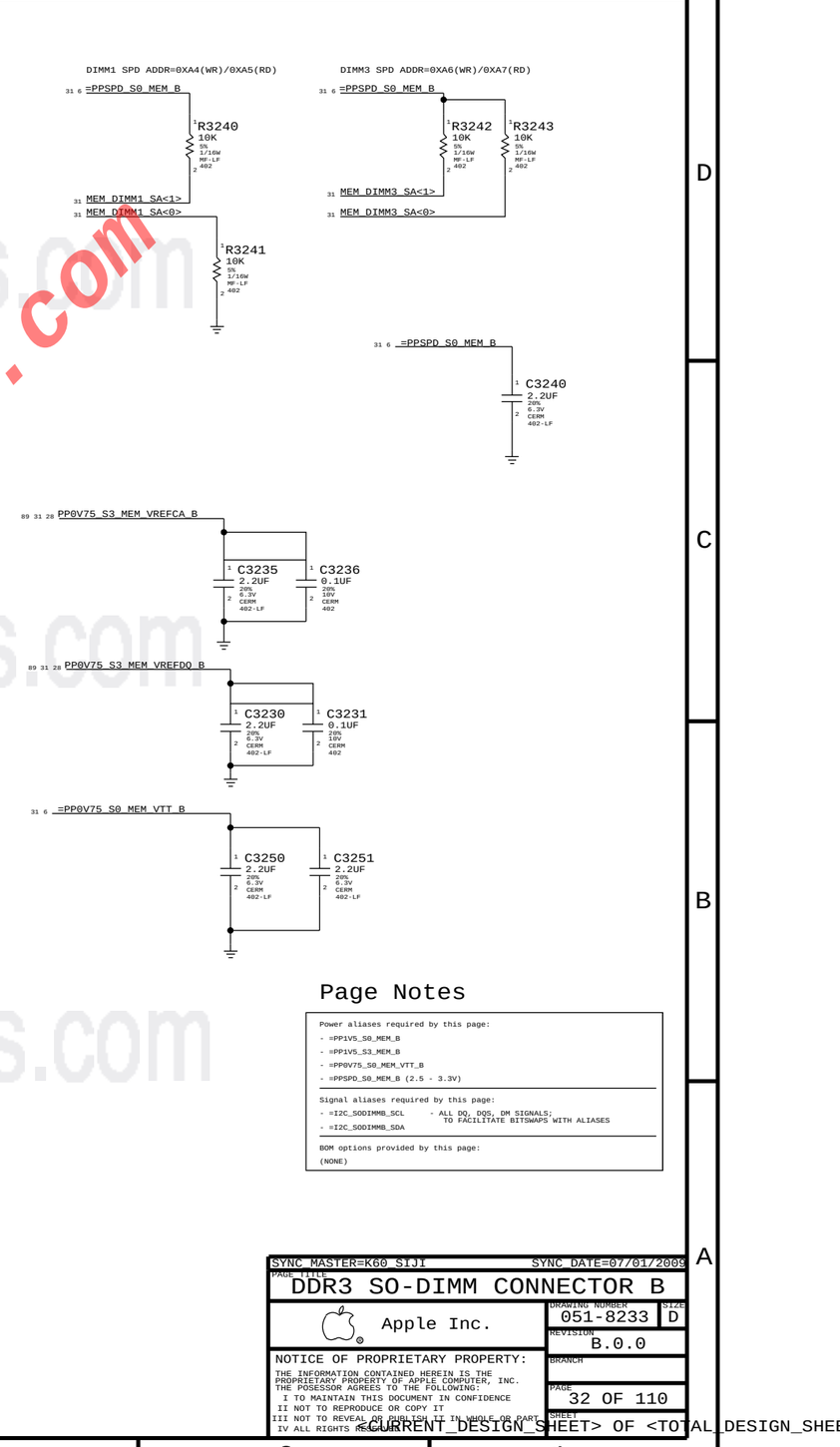

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA
- ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
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PAGE TITLE: DDR3 SO-DIMM CONNECTOR B

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D
REVISION: B.0.0
BRANCH:
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SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

DDR3 RESET Support

LFD CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.

S	R	CLK	D	Q	QB
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	POSEDGE	L	L	H
H	H	POSEDGE	H	H	L

	CPU_RESET_L	ISOLATE_L	MEM_RESET_L
S5	0	3.3V	0
S0	0	3.3V	0
S0	1.5V	3.3V	1.5V
S3	0	0	1.5V
S0	1.5V	3.3V	1.5V
S5	0	3.3V	0

CPU CHANNEL A DQS 0 -> DIMM A DQS 7

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>
MEM_A_DM<0>	MAKE_BASE=TRUE	=MEM_A_DM<7>
MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<57>
MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<56>
MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<58>
MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<59>
MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<60>
MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<61>
MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<62>
MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<63>

CPU CHANNEL A DQS 1 -> DIMM A DQS 6

MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>
MEM_A_DM<1>	MAKE_BASE=TRUE	=MEM_A_DM<6>
MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<49>
MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<52>
MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<51>
MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<50>
MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<48>
MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<53>
MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<55>
MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<54>

CPU CHANNEL A DQS 2 -> DIMM A DQS 5

MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>
MEM_A_DM<2>	MAKE_BASE=TRUE	=MEM_A_DM<5>
MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<40>
MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<45>
MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<46>
MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<47>
MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<41>
MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<44>
MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<43>
MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<42>

CPU CHANNEL A DQS 3 -> DIMM A DQS 4

MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>
MEM_A_DM<3>	MAKE_BASE=TRUE	=MEM_A_DM<4>
MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<37>
MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<33>
MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<35>
MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<34>
MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<36>
MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<32>
MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<38>
MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<39>

CPU CHANNEL A DQS 4 -> DIMM A DQS 3

MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>
MEM_A_DM<4>	MAKE_BASE=TRUE	=MEM_A_DM<3>
MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<28>
MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<29>
MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<27>
MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<31>
MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<25>
MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<24>
MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<26>
MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<30>

CPU CHANNEL A DQS 5 -> DIMM A DQS 2

MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>
MEM_A_DM<5>	MAKE_BASE=TRUE	=MEM_A_DM<2>
MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<17>
MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<16>
MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<22>
MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<23>
MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<21>
MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<20>
MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<18>
MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<19>

CPU CHANNEL A DQS 6 -> DIMM A DQS 1

MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>
MEM_A_DM<6>	MAKE_BASE=TRUE	=MEM_A_DM<1>
MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<12>
MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<13>
MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<10>
MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<15>
MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<8>
MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<9>
MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<11>
MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<14>

CPU CHANNEL A DQS 7 -> DIMM A DQS 0

MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>
MEM_A_DM<7>	MAKE_BASE=TRUE	=MEM_A_DM<0>
MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<5>
MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<4>
MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<3>
MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<2>
MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<1>
MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<0>
MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<7>
MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<6>

CPU CHANNEL B DQS 0 -> DIMM B DQS 7

MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>
MEM_B_DM<0>	MAKE_BASE=TRUE	=MEM_B_DM<7>
MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<61>
MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<60>
MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<62>
MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<63>
MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<56>
MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<57>
MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<58>
MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<59>

CPU CHANNEL B DQS 1 -> DIMM B DQS 6

MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>
MEM_B_DM<1>	MAKE_BASE=TRUE	=MEM_B_DM<6>
MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<51>
MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<54>
MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<53>
MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<52>
MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<48>
MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<49>
MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<50>
MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<55>

CPU CHANNEL B DQS 2 -> DIMM B DQS 5

MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>
MEM_B_DM<2>	MAKE_BASE=TRUE	=MEM_B_DM<5>
MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<45>
MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<40>
MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<42>
MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<47>
MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<44>
MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<41>
MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<46>
MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<43>

CPU CHANNEL B DQS 3 -> DIMM B DQS 4

MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>
MEM_B_DM<3>	MAKE_BASE=TRUE	=MEM_B_DM<4>
MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<32>
MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<39>
MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<37>
MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<38>
MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<35>
MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<34>
MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<36>
MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<33>

CPU CHANNEL B DQS 4 -> DIMM B DQS 3

MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>
MEM_B_DM<4>	MAKE_BASE=TRUE	=MEM_B_DM<3>
MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<28>
MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<24>
MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<31>
MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<30>
MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<29>
MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<25>
MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<27>
MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<26>

CPU CHANNEL B DQS 5 -> DIMM B DQS 2

MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>
MEM_B_DM<5>	MAKE_BASE=TRUE	=MEM_B_DM<2>
MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<18>
MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<20>
MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<23>
MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<22>
MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<19>
MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<21>
MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<17>
MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<16>

CPU CHANNEL B DQS 6 -> DIMM B DQS 1

MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>
MEM_B_DM<6>	MAKE_BASE=TRUE	=MEM_B_DM<1>
MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<8>
MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<14>
MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<10>
MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<11>
MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<9>
MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<15>
MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<12>
MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<13>

CPU CHANNEL B DQS 7 -> DIMM B DQS 0

MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>
MEM_B_DM<7>	MAKE_BASE=TRUE	=MEM_B_DM<0>
MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<2>
MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<1>
MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<3>
MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<7>
MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<4>
MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<5>
MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<6>
MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<0>

MEMORY CLOCK ALIASING

MEM_A_CLK_P<0>	MAKE_BASE=TRUE	=MEM_A_CLK_P<0>
MEM_A_CLK_N<0>	MAKE_BASE=TRUE	=MEM_A_CLK_N<0>
MEM_A_CLK_P<1>	MAKE_BASE=TRUE	=MEM_A_CLK_P<1>
MEM_A_CLK_N<1>	MAKE_BASE=TRUE	=MEM_A_CLK_N<1>
MEM_A_CLK_P<2>	MAKE_BASE=TRUE	=MEM_A_CLK_P<2>
MEM_A_CLK_N<2>	MAKE_BASE=TRUE	=MEM_A_CLK_N<2>
MEM_A_CLK_P<3>	MAKE_BASE=TRUE	=MEM_A_CLK_P<3>
MEM_A_CLK_N<3>	MAKE_BASE=TRUE	=MEM_A_CLK_N<3>
MEM_B_CLK_P<0>	MAKE_BASE=TRUE	=MEM_B_CLK_P<0>
MEM_B_CLK_N<0>	MAKE_BASE=TRUE	=MEM_B_CLK_N<0>
MEM_B_CLK_P<1>	MAKE_BASE=TRUE	=MEM_B_CLK_P<1>
MEM_B_CLK_N<1>	MAKE_BASE=TRUE	=MEM_B_CLK_N<1>
MEM_B_CLK_P<2>	MAKE_BASE=TRUE	=MEM_B_CLK_P<2>
MEM_B_CLK_N<2>	MAKE_BASE=TRUE	=MEM_B_CLK_N<2>
MEM_B_CLK_P<3>	MAKE_BASE=TRUE	=MEM_B_CLK_P<3>
MEM_B_CLK_N<3>	MAKE_BASE=TRUE	=MEM_B_CLK_N<3>

SYNC_MASTER=K60 SIJI SYNC_DATE=07/01/2009

PAGE TITLE: DDR3 SUPPORT AND BITSWAPS

Apple Inc.

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SIZE	D
REVISION	B.0.0
BRANCH	
PAGE	33 OF 110
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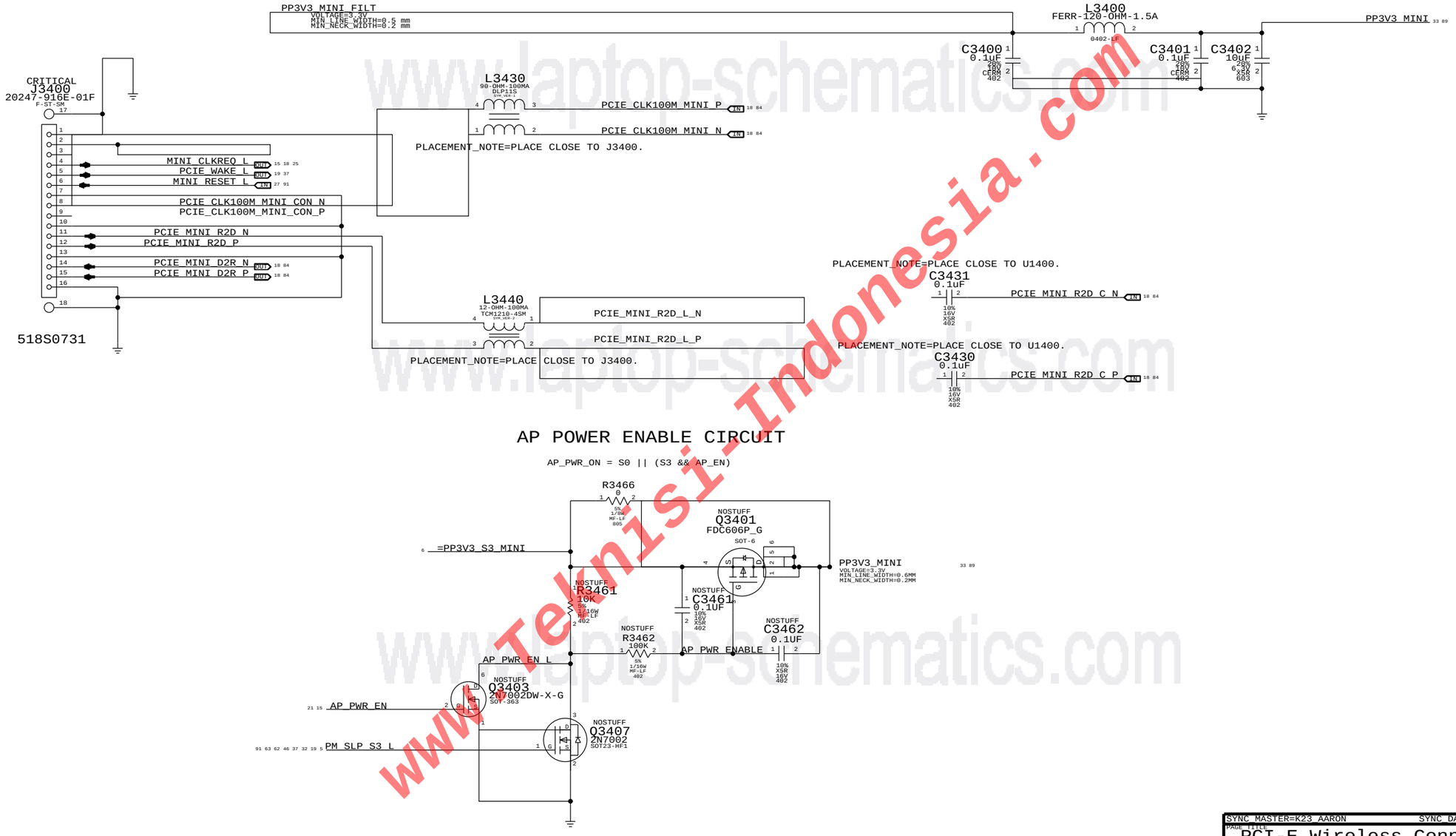

SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE
PCI-E Wireless Connector

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION B.0.0
BRANCH
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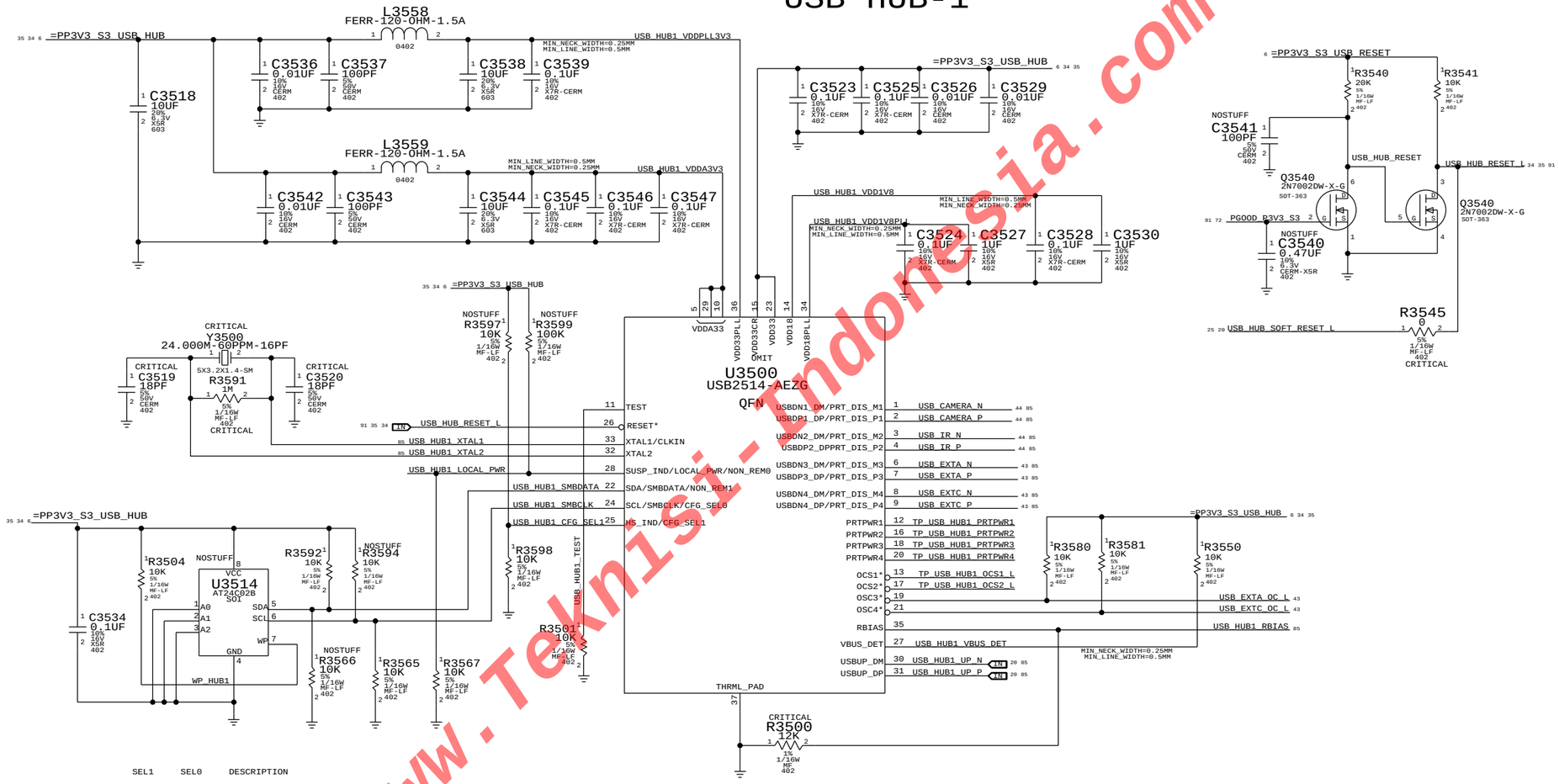
USB HUB-1



SEL1	SEL0	DESCRIPTION
DEFAULT K23F ==> 0	0	Internal Default with Self powered Operation
0	1	SMBUS Slave Config
1	0	Internal Default with Bus powered Operation
1	1	EEPROM Supported

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are Non removable
0	1	Port1 is non removable
DEFAULT K23F ==> 1	0	Port 1 and 2 are non removable
1	1	Port1,2 and 3 are non Removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U3500,U3600	CRITICAL	

SYNC_MASTER=K60_AARON SYNC_DATE=07/01/2009

PAGE TITLE: USB HUB 1

Apple Inc.

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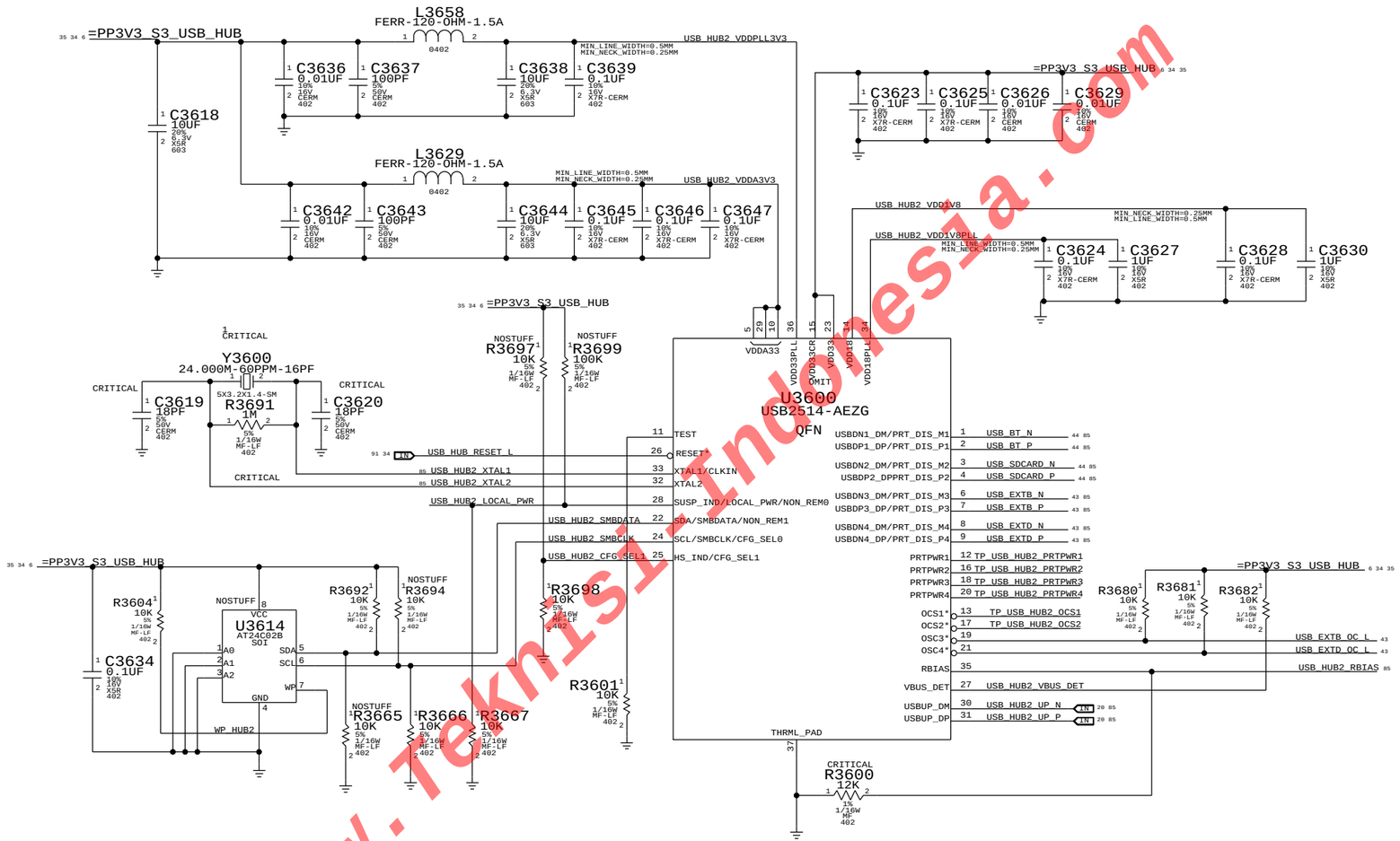
USB HUB-2



SYNC_MASTER=K60_AARON	SYNC_DATE=07/01/2009
PAGE TITLE	USB HUB 2
Apple Inc.	DRAWING NUMBER 051-8233 · SIZE D
	REVISION B.0.0
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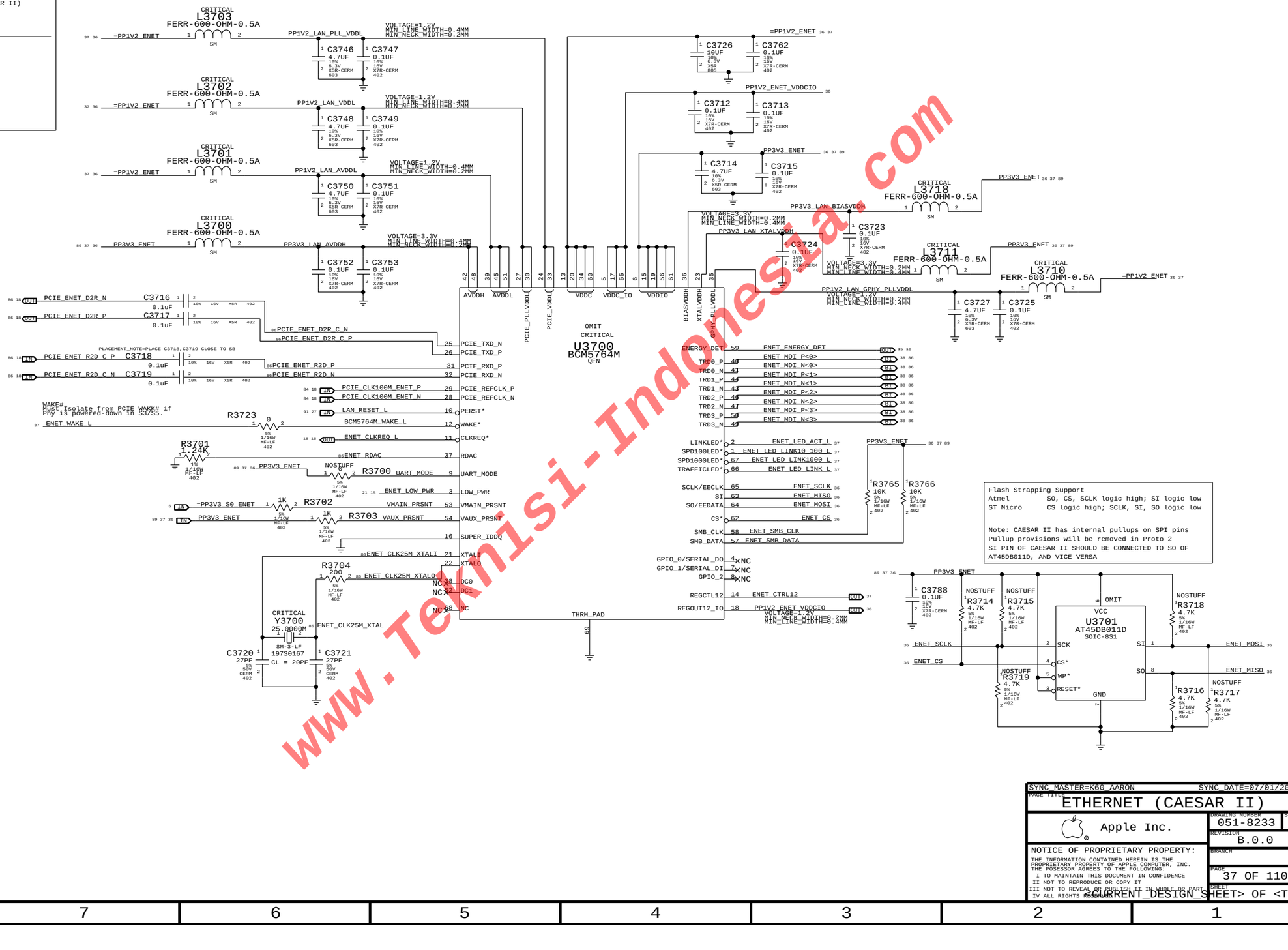
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- PP3V3_ENET (CAESAR II)
- =PP1V2_ENET



SYNC MASTER=K60_AARON SYNC DATE=07/01/2009

PAGE TITLE: ETHERNET (CAESAR II)

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

REVISION: B.0.0

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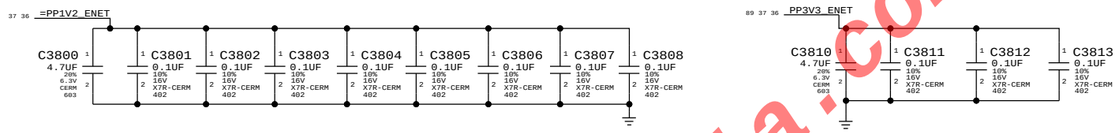
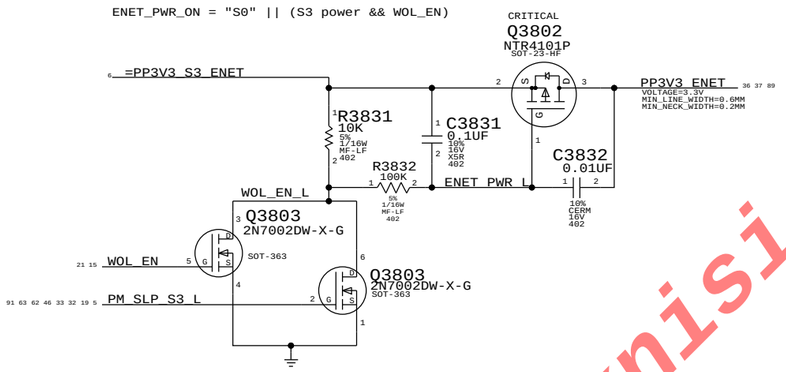
CAESAR II DECOUPLING

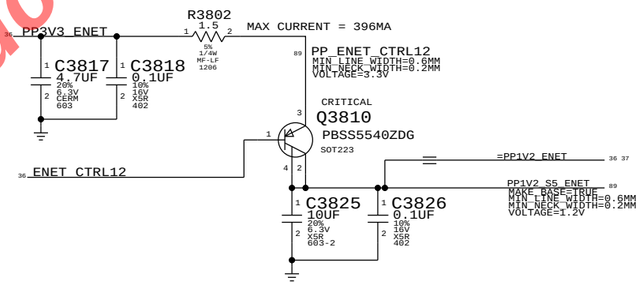


ENET POWER ENABLE CIRCUIT

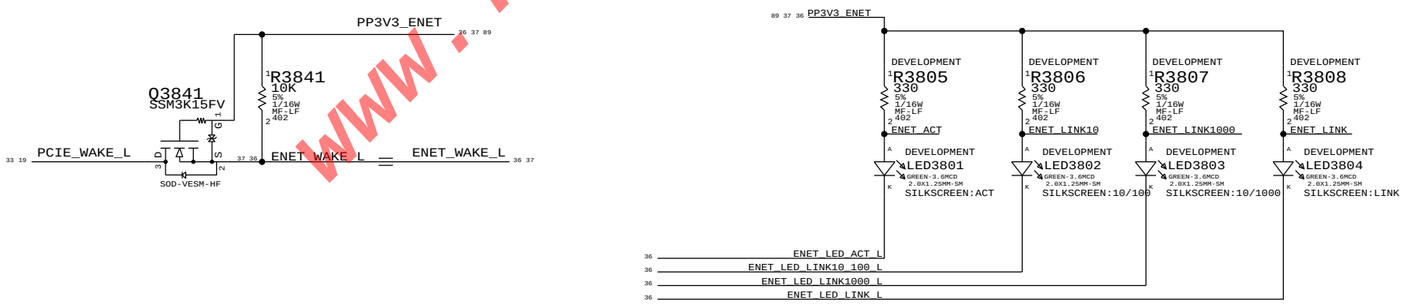
ENET_PWR_ON = "S0" || (S3 power && WOL_EN)



CAESAR II 1V2 RAIL SUPPLY



CAESAR II LED SUPPORT



SYNC_MASTER=K60_AARON SYNC_DATE=07/01/2009

PAGE TITLE: CAESAR II SUPPORT

Apple Inc.

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REVISION: B.0.0

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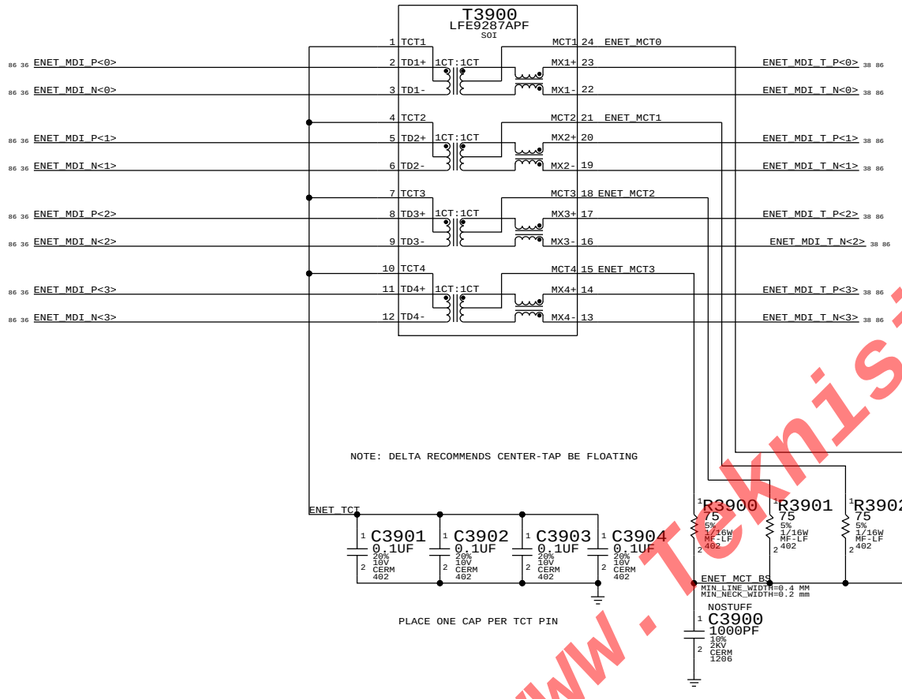

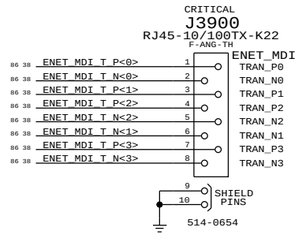

SYNC_MASTER=K60_AARON SYNC_DATE=07/01/2009

PAGE TITLE
ETHERNET CONNECTOR

Apple Inc.

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Power Aliases:

FW_FWPHY nets are PHY power, and for multi-port systems must come from bus power.

FWRS0_FWXIO nets are OHCI/PCIe power, and can be S0.

For single-port systems, all FW power should be tied together and powered by S0 or by the 5K pull-down device detect circuit.

PCI EXPRESS

1394B OHCI & PHY

U4100 XIO2213B BGA

OMIT CRITICAL

Single-port: PC[0:2] = '000'

Multiple-ports: PC[0:2] = '100'

Alias =FWPHY_PC0 as appropriate

Unused Ports:

TP/NC TPBIASx

TP/NC TPAx_P/TPAx_N

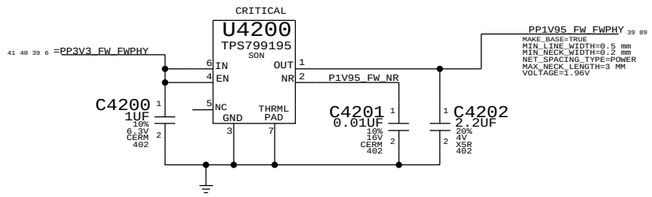
Ground TPBx_P/TPBx_N

DS2 hard-strapped to 1, page assumes no more than 2 FW800 connectors

Strap DSx high on unused ports.

SYNC_MASTER=K23_AARON	SYNC_DATE=07/16/2009
PAGE_TITLE: FireWire LLC/PHY (XIO2213B)	
Apple Inc.	DRAWING NUMBER: 051-8233 SIZE: D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	REVISION: B.0.0 BRANCH PAGE: 41 OF 110 SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

1394 PHY 1.95V SUPPLY



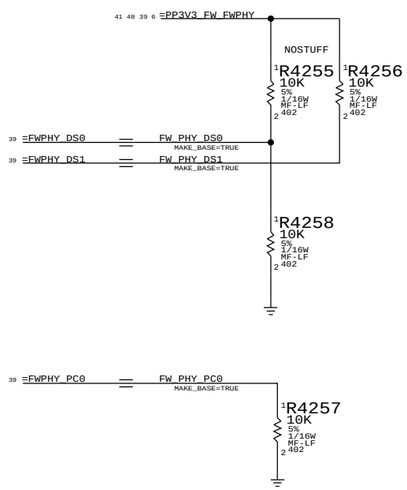
FireWire Aliases For Connectivity

39 =FW_CLKREQ_L = FW_CLKREQ_L 15 18 25 (MAKE_BASE=TRUE)

39 =FW_PME_L = FW_PME_L 15 21 (MAKE_BASE=TRUE)

39 =PPVP_FW_PHY_CPS = PPVP_FW_PHY_CPS 41 89 (MAKE_BASE=TRUE)

1394 PHY STRAPPING OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

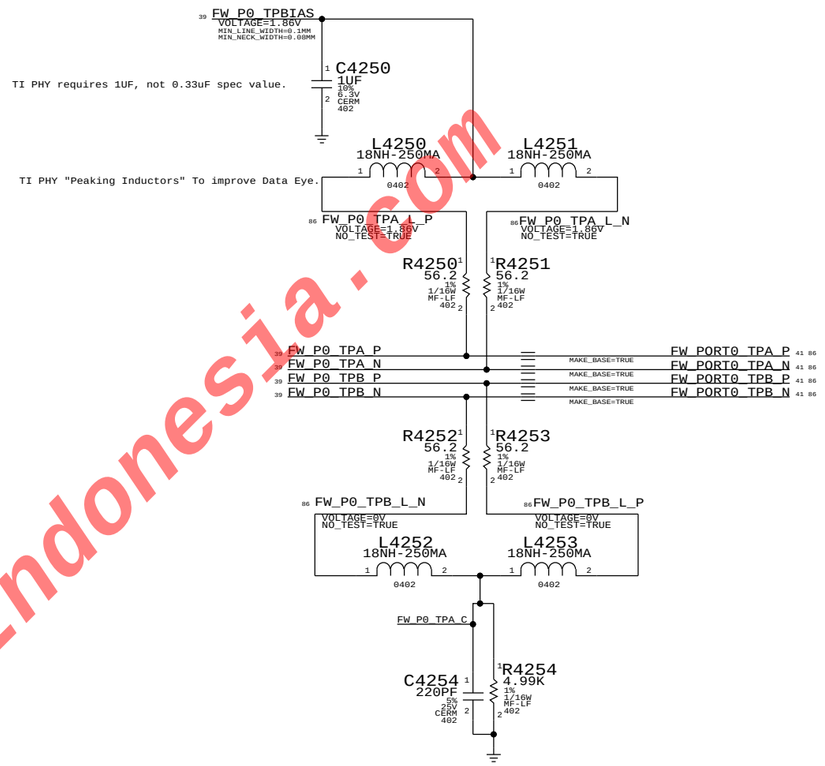
iMacs are now one port only and have Power Code "000"

Termination

Place close to FireWire PHY

TI PHY requires 1UF, not 0.33uF spec value.

TI PHY "Peaking Inductors" To improve Data Eye.



2ND & 3RD TPA/TPB PAIR UNUSED

39 FW_P1_TPBIAS = NC_FW_PORT1_TPBIAS (MAKE_BASE=TRUE, NO_TEST=TRUE)

86 39 FW_P1_TPA_P = NC_FW_PORT1_TPA_P (MAKE_BASE=TRUE, NO_TEST=TRUE)

86 39 FW_P1_TPA_N = NC_FW_PORT1_TPA_N (MAKE_BASE=TRUE, NO_TEST=TRUE)

39 FW_P2_TPBIAS = NC_FW_PORT2_TPBIAS (MAKE_BASE=TRUE, NO_TEST=TRUE)

86 39 FW_P2_TPA_P = NC_FW_PORT2_TPA_P (MAKE_BASE=TRUE, NO_TEST=TRUE)

86 39 FW_P2_TPA_N = NC_FW_PORT2_TPA_N (MAKE_BASE=TRUE, NO_TEST=TRUE)

SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE

FW: 1394B MISC

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

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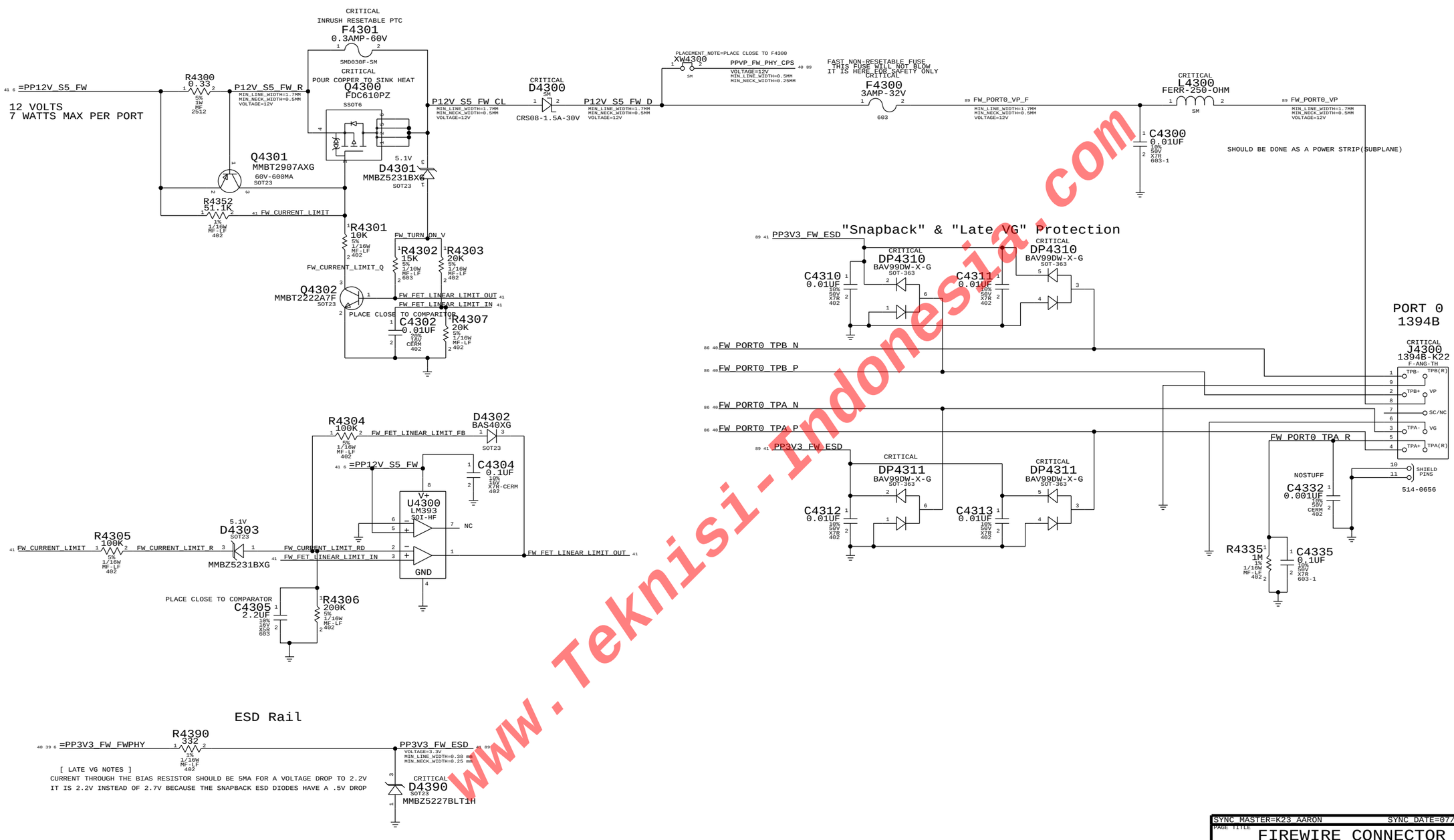
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE
FIREWIRE CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION B.0.0
BRANCH
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SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

SATA PORT A0 FOR HDD

SILKSCREEN:HDD

CRITICAL
J4510
EP00-081-91
M-ST-SM

518S0251

SATA_HDD_R2D_P	C4510 0.01UF	SATA_HDD_R2D_C_P	IN
SATA_HDD_R2D_N	C4511 0.01UF	SATA_HDD_R2D_C_N	IN
SATA_HDD_D2R_C_N	C4515 0.01UF	SATA_HDD_D2R_N	OUT
SATA_HDD_D2R_C_P	C4516 0.01UF	SATA_HDD_D2R_P	OUT

C4510–C4516: 0.01UF, 10% 16V CERM 402

SATA Activity LED

=PP3V3_S0_SATALED

DEVELOPMENT
R4599 330 5% 1/10W MF-LF 603

SATALED_R_L

DEVELOPMENT
DS4599
GREEN-3.6MCD
2.0X1.25MM-SM

SILK_PART=SATA ACTIVE

PCH_SATALED_L

SATALED_L
MAKE_BASE=TRUE

SATA PORT A1 FOR SLIMLINE ODD

518-0361
SILKSCREEN:ODD
J4520
1735574
M-ST-TH

SATA_ODD_R2D_P	C4520 0.01UF	SATA_ODD_R2D_C_P	IN
SATA_ODD_R2D_N	C4521 0.01UF	SATA_ODD_R2D_C_N	IN
SATA_ODD_D2R_C_N	C4522 0.01UF	SATA_ODD_D2R_N	OUT
SATA_ODD_D2R_C_P	C4523 0.01UF	SATA_ODD_D2R_P	OUT

C4520–C4523: 0.01UF, 10% 16V CERM 402

PP5V_S0_SATA_FET
NET_PHYSICAL_TYPE=POWER

C4524 1UF 10% 6.3V CERM 402
C4525 1UF 10% 6.3V CERM 402

=PP3V3_S0_ODD

R4520 3.3K 5% 1/10W MF-LF 603

SMC_ODD_DETECT

R4550 0 5% 1/10W MF-LF 805

Q4500 NOSTUFF
TPCP8102
23V1K-SM

=PP5V_S0_SATA

NOSTUFF R4501 100K 5% 1/10W MF-LF 402

NOSTUFF C4501 0.068UF 10% 10V CERM 402

NOSTUFF C4500 0.01UF 10% 16V CERM 402

ODD_PWR_LSGV_L

NOSTUFF R4500 100K 5% 1/10W MF-LF 402

ODD_PWR_SS

=PP3V3_S0_ODD

NOSTUFF R4502 100K 5% 1/10W MF-LF 402

ODD_PWR_EN

Q4502
2N7002DW-X-G
SOT-363

NOSTUFF
Q4502
2N7002DW-X-G
SOT-363

ODD_PWR_EN_L

ODD PWR CONTROL

SATA PORT A2 FOR SSD

NOSTUFF
CRITICAL
J4530
EP00-081-91
M-ST-SM

518S0251

SATA_SSD_R2D_P	C4530 0.01UF	SATA_SSD_R2D_C_P	IN
SATA_SSD_R2D_N	C4531 0.01UF	SATA_SSD_R2D_C_N	IN
SATA_SSD_D2R_C_N	C4532 0.01UF	SATA_SSD_D2R_N	OUT
SATA_SSD_D2R_C_P	C4533 0.01UF	SATA_SSD_D2R_P	OUT

C4530–C4533: NOSTUFF, 0.01UF, 10% 16V CERM 402

SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE: SATA Connectors

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D
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SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

USB/SMC DEBUG MUX

=PP3V3_G3H_SMCUSBMUX

=PP5V_S3_USB

USB_PWR_ENA_L

PM_EN_USB_PWR

PORT 3

U4601 TPS2060 MSOP
USB_EXTC_OC_L, USB_EXTD_OC_L

R4600 10K 5% 1/16W MF-LF 402

C4605 0.1UF 20% 16V CERM 402

C4606 150UF 20% 6.3V POLY-TANT CASE-D2-SM

C4621 0.1UF 20% 16V CERM 402

C4631 0.1UF 20% 16V CERM 402

Q4600 2N7002 SOT23-HF

C4650 0.1UF 20% 16V CERM 402

U4650 MOJOMUX PI3USB102ZLE TQFN
SMC_RX_L, SMC_TX_L, USB_EXTD_P, USB_EXTD_N

USB_DEBUGPRT_EN_L
SEL=0: CHOOSE SMC
SEL=1: CHOOSE USB

R4651 PRODUCTION 0 5% 1/10W MF-LF 402

R4652 PRODUCTION 0 5% 1/10W MF-LF 402

USB_D_MUXED_N, USB_D_MUXED_P

L4630 FERR-250-OHM SM

C4630 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)

PP5V_USB2_PORT3
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM

PP5V_USB2_PORT3_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM

L4631 120-OHM-90MA DLP0NS

USB_PORT3_N, USB_PORT3_P

J4630 USB-K22 F-ANG-TH
VDD, D-, D+, GND
VBUS, DATA-, DATA+, GND
514-0659

D4630 RCLAMP0502N SLP1210N6
VBUS, GND, NC, IO

PORT 2

U4600 TPS2060 MSOP
USB_EXTA_OC_L, USB_EXTB_OC_L

C4601 0.1UF 20% 16V CERM 402

C4602 150UF 20% 6.3V POLY-TANT CASE-D2-SM

C4603 0.1UF 20% 16V CERM 402

C4611 0.1UF 20% 16V CERM 402

L4610 FERR-250-OHM SM

C4610 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)

PP5V_USB2_PORT1
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM

PP5V_USB2_PORT1_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM

L4620 FERR-250-OHM SM

C4620 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)

PP5V_USB2_PORT2
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM

PP5V_USB2_PORT2_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM

L4611 120-OHM-90MA DLP0NS

USB_EXTB_N, USB_EXTB_P, USB_PORT1_N, USB_PORT1_P

J4610 USB-K22 F-ANG-TH1
VDD, D-, D+, GND
VBUS, DATA-, DATA+, GND
514-0672

D4610 RCLAMP0502N SLP1210N6
VBUS, GND, NC, IO

L4621 120-OHM-90MA DLP0NS

USB_EXTC_N, USB_EXTC_P, USB_PORT2_N, USB_PORT2_P

J4620 USB-K22 F-ANG-TH
VDD, D-, D+, GND
VBUS, DATA-, DATA+, GND
514-0659

D4620 RCLAMP0502N SLP1210N6
VBUS, GND, NC, IO

PORT 0

L4600 FERR-250-OHM SM

C4600 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)

PP5V_USB2_PORT0
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM

PP5V_USB2_PORT0_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM

L4601 120-OHM-90MA DLP0NS

USB_EXTA_N, USB_EXTA_P, USB_PORT0_N, USB_PORT0_P

J4600 USB-K22 F-ANG-TH1
VDD, D-, D+, GND
VBUS, DATA-, DATA+, GND
514-0672

D4600 RCLAMP0502N SLP1210N6
VBUS, GND, NC, IO

SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE
EXTERNAL USB CONNECTORS

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
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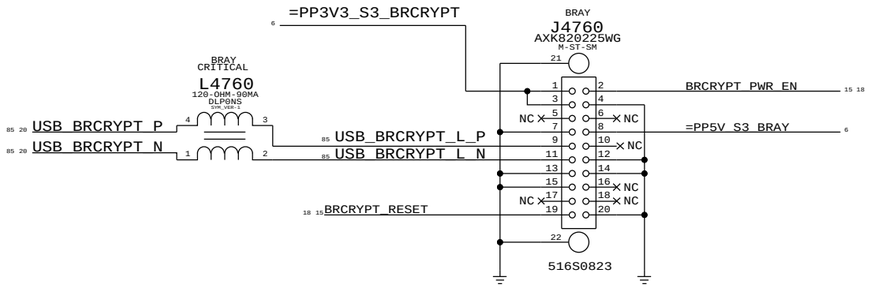
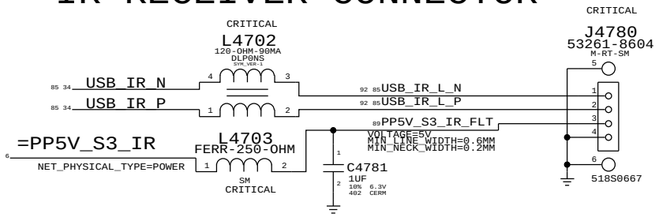
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

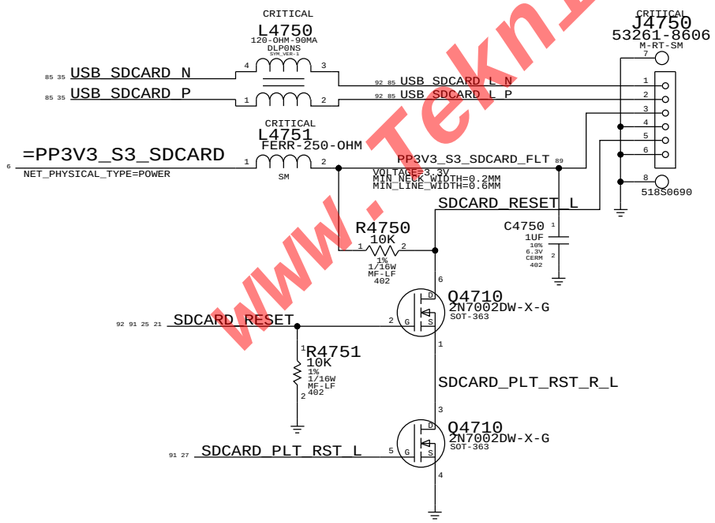
BLURAY DECRYPTOR CONN & FLTR



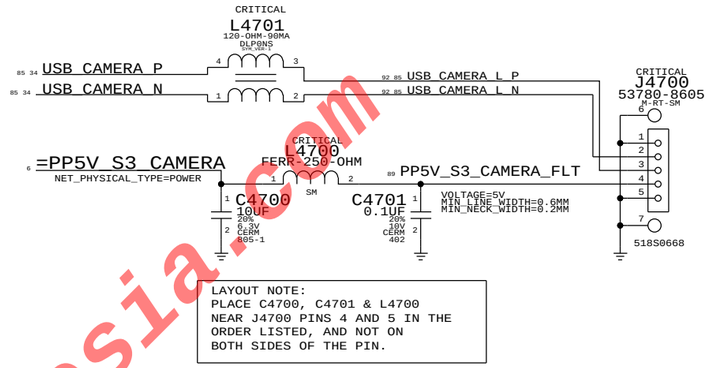
IR RECEIVER CONNECTOR



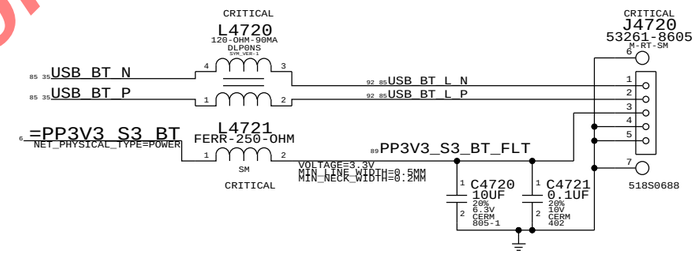
SD Card Reader Board Connector



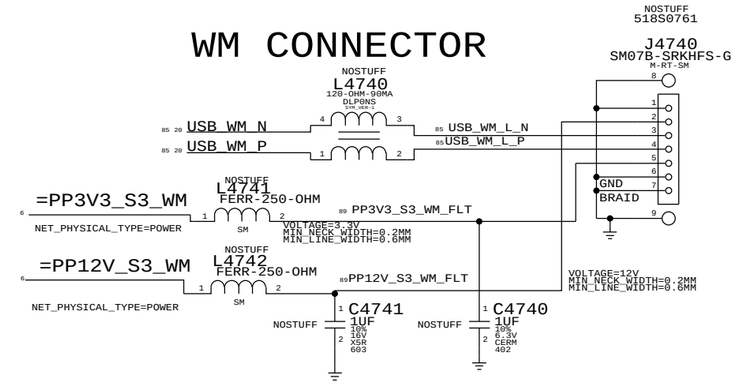
CAMERA CONNECTOR & FILTER



K37L (BLUETOOTH) CONNECTOR



WM CONNECTOR



SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2005

PAGE TITLE: Internal USB Connections

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

REVISION: B.0.0

BRANCH:

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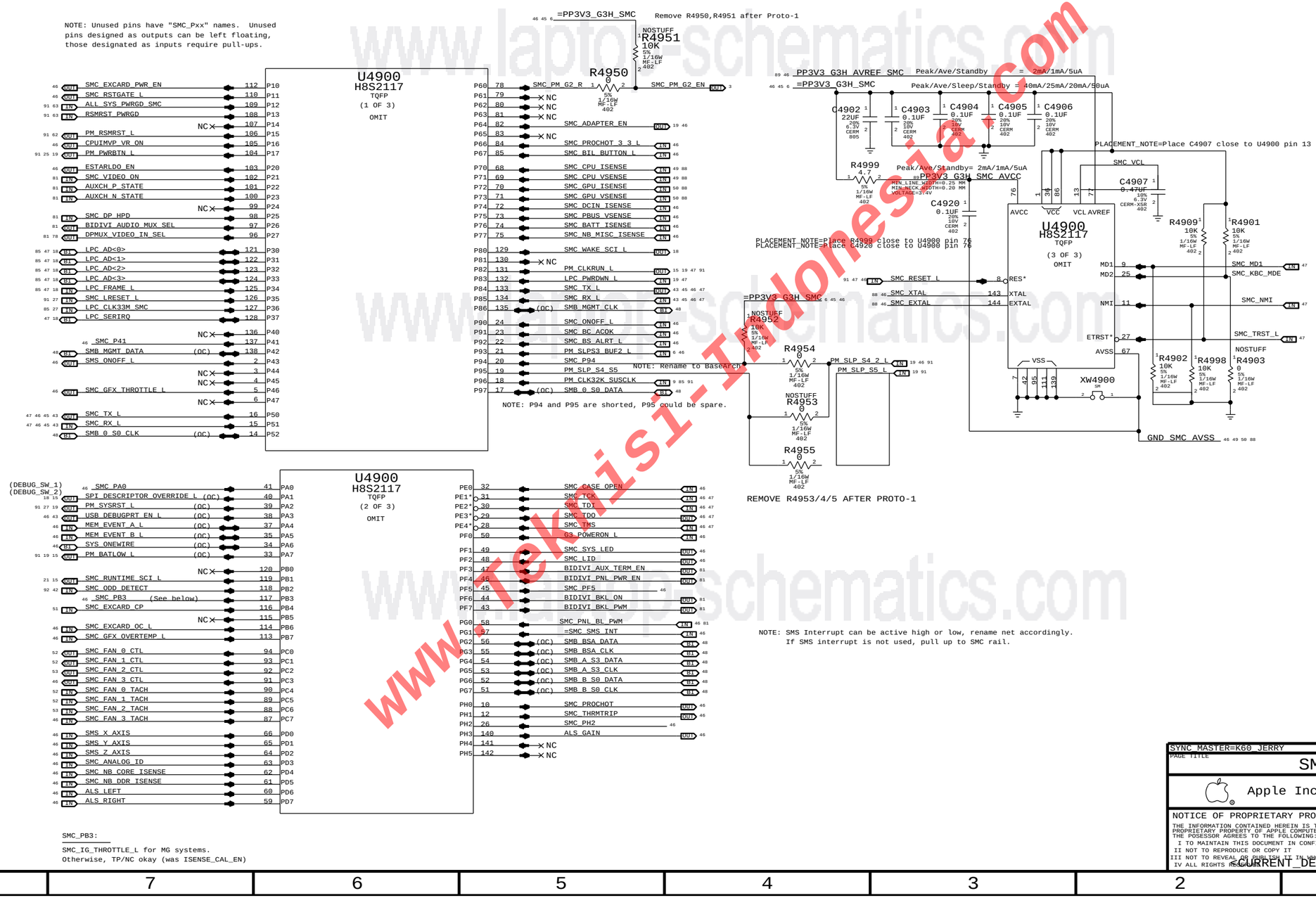
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>


NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.
U4900
H8S2117
TQFP
(1 OF 3)
OMIT
SMC_EXCARD_PWR_EN
SMC_RSTGATE_L
ALL_SYS_PWRGD_SMC
RSMRST_PWRGD
PM_RSMRST_L
CPUIMVP_VR_ON
PM_PWRBTN_L
ESTARLDO_EN
SMC_VIDEO_ON
AUXCH_P_STATE
AUXCH_N_STATE
SMC_DP_HPD
BIDIVI_AUDIO_MUX_SEL
DPMUX_VIDEO_IN_SEL
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
LPC_FRAME_L
SMC_LRESET_L
LPC_CLK33M_SMC
LPC_SERIRQ
SMC_P41
SMB_MGMT_DATA (OC)
SMS_ONOFF_L
SMC_GFX_THROTTLE_L
SMC_TX_L
SMC_RX_L
SMB_0_S0_CLK (OC)
=PP3V3_G3H_SMC
Remove R4950,R4951 after Proto-1
R4951 10K
R4950 0
SMC_PM_G2_R
SMC_PM_G2_EN
SMC_ADAPTER_EN
SMC_PROCHOT_3_3_L
SMC_BIL_BUTTON_L
SMC_CPU_ISENSE
SMC_CPU_VSENSE
SMC_GPU_ISENSE
SMC_GPU_VSENSE
SMC_DCIN_ISENSE
SMC_PBUS_VSENSE
SMC_BATT_ISENSE
SMC_NB_MISC_ISENSE
SMC_WAKE_SCI_L
PM_CLKRUN_L
LPC_PWRDWN_L
SMC_TX_L
SMC_RX_L
SMB_MGMT_CLK
SMC_ONOFF_L
SMC_BC_ACOK
SMC_BS_ALRT_L
PM_SLPS3_BUF2_L
SMC_P94
PM_SLP_S4_S5
PM_CLK32K_SUSCLK
SMB_0_S0_DATA
NOTE: P94 and P95 are shorted, P95 could be spare.
NOTE: Rename to BaseArch
PP3V3_G3H_AVREF_SMC
Peak/Ave/Standby = 2mA/1mA/5uA
=PP3V3_G3H_SMC
Peak/Ave/Sleep/Standby = 40mA/25mA/20mA/50uA
C4902 22UF
C4903 0.1UF
C4904 0.1UF
C4905 0.1UF
C4906 0.1UF
R4999 4.7
Peak/Ave/Standby= 2mA/1mA/5uA
PP3V3_G3H_SMC_AVCC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.4V
C4920 0.1UF
PLACEMENT_NOTE=Place C4907 close to U4900 pin 13
C4907 0.47UF
SMC_VCL
PLACEMENT_NOTE=Place R4900 close to U4900 pin 76
PLACEMENT_NOTE=Place C4920 close to U4900 pin 76
U4900
H8S2117
TQFP
(3 OF 3)
OMIT
AVCC
VCC
VCL
AVREF
R4909 10K
R4901 10K
SMC_RESET_L
SMC_XTAL
SMC_EXTAL
RES*
XTAL
EXTAL
MD1
MD2
NMI
ETRST*
AVSS
SMC_MD1
SMC_KBC_MDE
SMC_NMI
SMC_TRST_L
VSS
XW4900
R4902 10K
R4998 10K
R4903 0
NOSTUFF
GND_SMC_AVSS
R4952 10K
R4954 0
R4953 0
R4955 0
PM_SLP_S4_2_L
PM_SLP_S5_L
REMOVE R4953/4/5 AFTER PROTO-1
U4900
H8S2117
TQFP
(2 OF 3)
OMIT
SMC_PA0
SPI_DESCRIPTOR_OVERRIDE_L (OC)
PM_SYSRST_L (OC)
USB_DEBUGPRT_EN_L (OC)
MEM_EVENT_A_L (OC)
MEM_EVENT_B_L (OC)
SYS_ONEWIRE (OC)
PM_BATLOW_L (OC)
SMC_RUNTIME_SCI_L
SMC_ODD_DETECT
SMC_PB3 (See below)
SMC_EXCARD_CP
SMC_EXCARD_OC_L
SMC_GFX_OVERTEMP_L
SMC_FAN_0_CTL
SMC_FAN_1_CTL
SMC_FAN_2_CTL
SMC_FAN_3_CTL
SMC_FAN_0_TACH
SMC_FAN_1_TACH
SMC_FAN_2_TACH
SMC_FAN_3_TACH
SMS_X_AXIS
SMS_Y_AXIS
SMS_Z_AXIS
SMC_ANALOG_ID
SMC_NB_CORE_ISENSE
SMC_NB_DDR_ISENSE
ALS_LEFT
ALS_RIGHT
SMC_CASE_OPEN
SMC_TCK
SMC_TDI
SMC_TDO
SMC_TMS
G3_POWERON_L
SMC_SYS_LED
SMC_LID
BIDIVI_AUX_TERM_EN
BIDIVI_PNL_PWR_EN
SMC_PF5
BIDIVI_BKL_ON
BIDIVI_BKL_PWM
SMC_PNL_BL_PWM
=SMC_SMS_INT
SMB_BSA_DATA
SMB_BSA_CLK
SMB_A_S3_DATA
SMB_A_S3_CLK
SMB_B_S0_DATA
SMB_B_S0_CLK
SMC_PROCHOT
SMC_THRMTRIP
SMC_PH2
ALS_GAIN
NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.
SMC_PB3:
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)
SYNC_MASTER=K60_JERRY
SYNC_DATE=07/01/2005
PAGE TITLE
SMC
Apple Inc.
DRAWING NUMBER 051-8233
SIZE D
REVISION B.0.0
BRANCH
PAGE 49 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>
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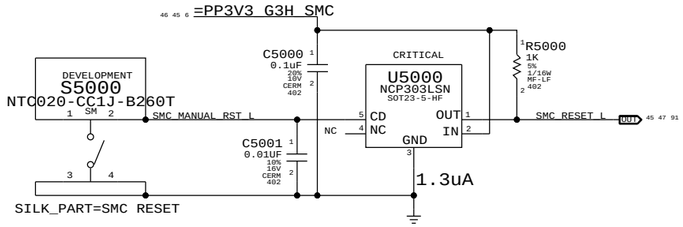
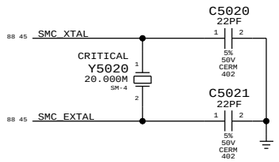
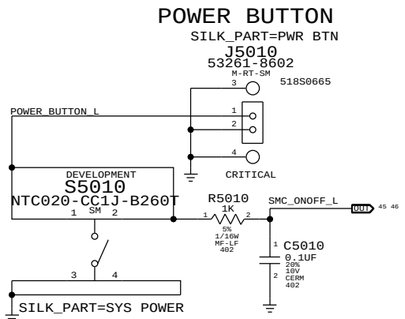
SMC Reset Button / Brownout Detect



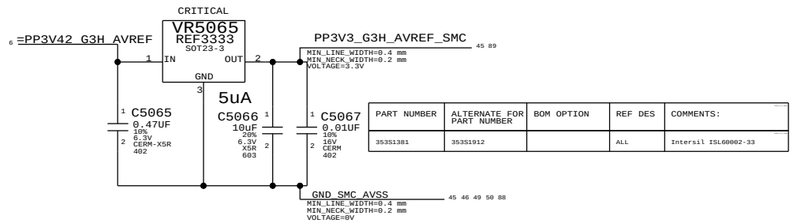
SMC Crystal Circuit



POWER BUTTON

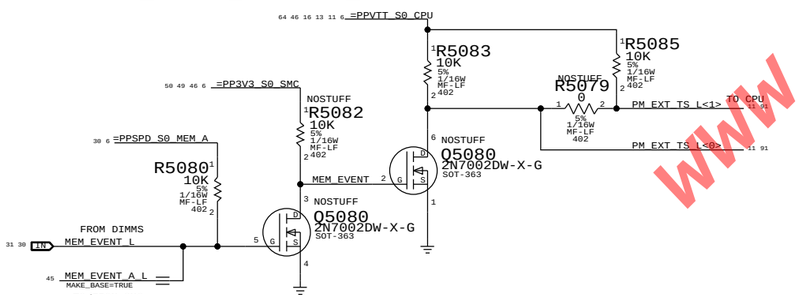


SMC AVREF Supply

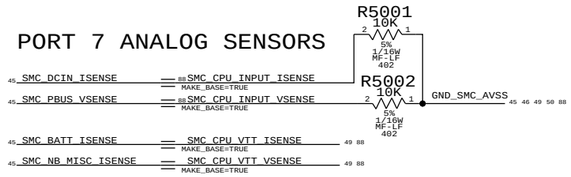


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

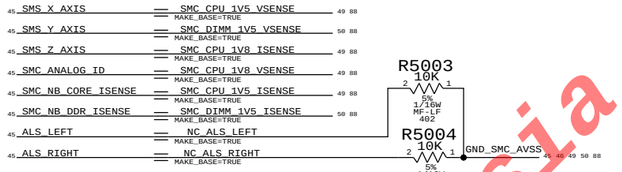
PM_EXTTS_L / MEM_EVENT LEVEL SHIFTING



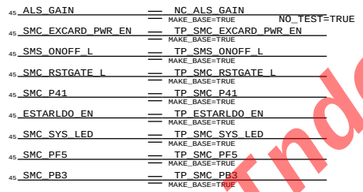
PORT 7 ANALOG SENSORS



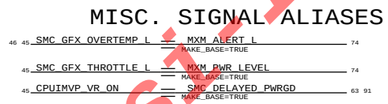
PORT D ANALOG SENSORS (INTERNAL PULLUPS)



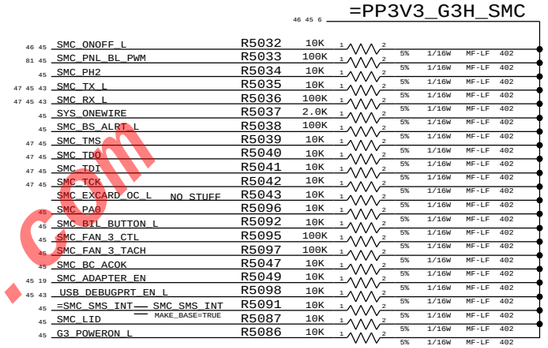
UNUSED TP/NC ALIASES



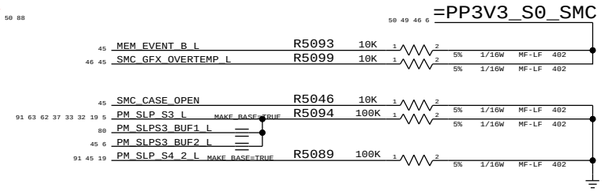
MISC. SIGNAL ALIASES



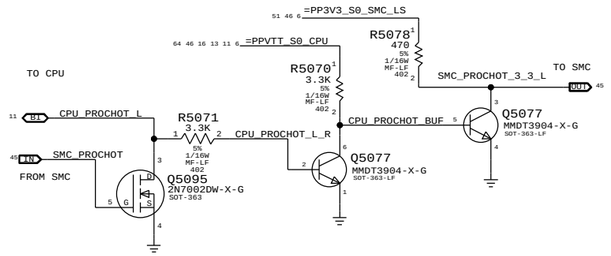
=PP3V3_G3H_SMC



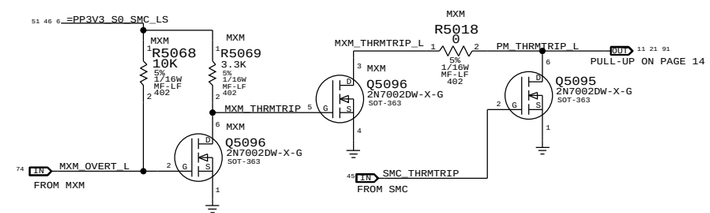
=PP3V3_S0_SMC



SMC PROCHOT 3.3V LEVEL SHIFTING

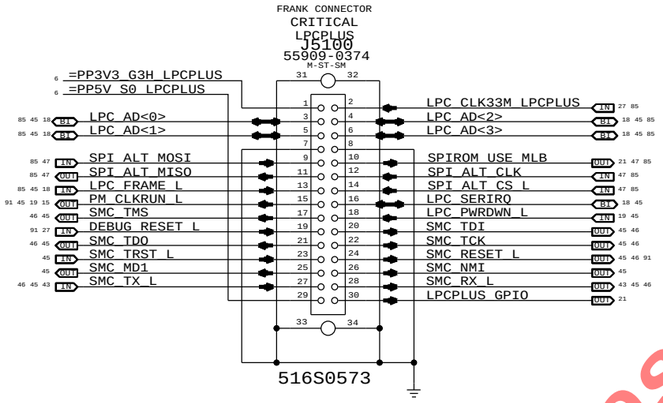


SMC & MXM THERMTRIP LEVEL SHIFTING

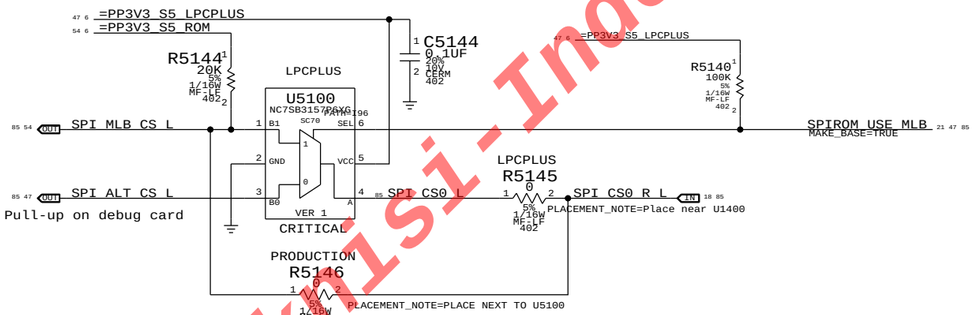


SYNC_MASTER=K60_JERRY	SYNC_DATE=07/01/2009
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER 051-8233 · SIZE D · REVISION B.0.0 · BRANCH · PAGE 50 OF 110 · SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

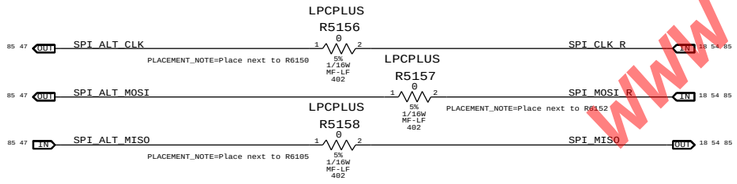
LPC+SPI Connector



Alternate SPI ROM Support



SPI Bus Series Resistance Option



SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

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PCH "SMBUS" CONNECTIONS

=PP3V3_S3_SMBUS

PCH
U1800
(MASTER)

88 18 SMBUS_PCH_CLK
MAKE_BASE=TRUE
88 18 SMBUS_PCH_DATA
MAKE_BASE=TRUE

NOSTUFF R5200 6.8K 5% 1/16W MF-LF 402
R5201 6.8K 5% 1/16W MF-LF 402

MEMORY A VREF
U2900
(WRITE: 0X7C READ: 0X7D)
=I2C_VREFMRGN_A_SCL 28
=I2C_VREFMRGN_A_SDA 28

MEMORY B VREF
U2910
(WRITE: 0X5C READ: 0X5D)
=I2C_VREFMRGN_B_SCL 28
=I2C_VREFMRGN_B_SDA 28

91 72 63 PGOOD_P3V3_S0

NOSTUFF Q5200 SI2302ADSE3 SOT23-3-HF
R5211 0 5% 1/16W MF-LF 402

R5210 0 5% 1/16W MF-LF 402

NOSTUFF Q5201 SI2302ADSE3 SOT23-3-HF

MEMORY A DIMMS
J3100-A/B
(Write: 0xA0 Read: 0xA1)
(WRITE: 0XA2 READ: 0XA5)
=I2C_SODIMMA_SCL 30
=I2C_SODIMMA_SDA 30

MEMORY B DIMMS
J3200-A/B
(WRITE: 0XA4 READ: 0XA3)
(WRITE: 0XA6 READ: 0XA7)
=I2C_SODIMMB_SCL 31
=I2C_SODIMMB_SDA 31

MIKEY
U6800
(WRITE: 0X72 READ: 0X73)
=I2C_AUDIO_SCL 61
=I2C_AUDIO_SDA 61

48 6 =PP3V3_S0_SMBUS

R5208 3.3K 5% 1/16W MF-LF 402
R5209 3.3K 5% 1/16W MF-LF 402

XDP
J2500/J2550
(MASTER)
25 =SMBUS_XDP_SCL
25 =SMBUS_XDP_SDA
88 SMBUS_PCH_S0_CLK
MAKE_BASE=TRUE
88 SMBUS_PCH_S0_DATA
MAKE_BASE=TRUE

CK505
U2600
(WRITE: 0XD2 READ: 0XD3)
=SMBUS_CK505_SCL 26
=SMBUS_CK505_SDA 26

PCH "SML 1" CONNECTIONS

48 6 =PP3V3_S0_SMBUS

PCH
U1800
(SLAVE)
(WRITE: 0X90 READ: 0X91)
88 18 SML_PCH_1_CLK
MAKE_BASE=TRUE
88 18 SML_PCH_1_DATA
MAKE_BASE=TRUE

NOSTUFF R5204 8.2K 5% 1/16W MF-LF 402
R5205 8.2K 5% 1/16W MF-LF 402

R5206 0 5% 1/16W MF-LF 402

R5207 0 5% 1/16W MF-LF 402

PCH "SML 0" CONNECTIONS

48 6 =PP3V3_S0_SMBUS

PCH
U1800
(MASTER)
88 18 SML_PCH_0_CLK
MAKE_BASE=TRUE
88 18 SML_PCH_0_DATA
MAKE_BASE=TRUE

R5202 8.2K 5% 1/16W MF-LF 402
R5203 8.2K 5% 1/16W MF-LF 402

SMC "B" SMBus Connections

6 =PP3V3_S0_SMBUS_SMC_B_S0

SMC
U4900
(MASTER)
45 SMB_B_S0_CLK
45 SMB_B_S0_DATA
88 SMBUS_SMC_B_S0_SCL
MAKE_BASE=TRUE
88 SMBUS_SMC_B_S0_SDA
MAKE_BASE=TRUE

R5260 2.2K 5% 1/16W MF-LF 402
R5261 2.2K 5% 1/16W MF-LF 402

REMOTE TEMPS
EMC1047-2, U5500, SEE TABLE
(WRITE: 0X90 READ: 0X91)
=SMB_REMOTE_TEMP_SCL 51
=SMB_REMOTE_TEMP_SDA 51

EMC1047-2 HEX DIODE SENSOR

DIODE	FUNCTION
1	ODD TEMP
2	LCD TEMP
3	AMBIENT TEMP
4	CPU HEATSINK
5	MXM HEATSINK

AC/DC PS TEMPS
EMC1403-[1,2]: ACDC THRU J600
(WRITE: 0X98 OR 0X9A, READ: 0X99 OR 0X9B)
3 SENSE POINTS - PRIMARY, SECONDARY, AMB
=SMB_ACDC_SCL 6
=SMB_ACDC_SDA 6

AC/DC PS POWER
INA219: ACDC THRU J600
(WRITE: 0X80, READ: 0X81))
OUTPUT VOLTAGE, CURRENT, POWER

SMC "0" SMBus Connections

6 =PP3V3_S0_SMBUS_SMC_0_S0

SMC
U4900
(MASTER)
45 SMB_0_S0_CLK
45 SMB_0_S0_DATA
88 SMBUS_SMC_0_S0_SCL
MAKE_BASE=TRUE
88 SMBUS_SMC_0_S0_SDA
MAKE_BASE=TRUE

R5250 4.7K 5% 1/16W MF-LF 402
R5251 4.7K 5% 1/16W MF-LF 402

MXM TEMP
GPU ON CARD - J8400
NV INSIDE (WRITE: 0X9E READ: 0X9F)
MXM CARD (WRITE: 0X98 READ: 0X99)
=SMB_MXM_THRM_SCL 74
=SMB_MXM_THRM_SDA 74

Also reserve 0x56 and 0x32 per spec

DIE TEMPS
EMC1402-2: U5535
(WRITE: 0X9A READ: 0X9B)
=SMB_CPU_THRM_SCL 51
=SMB_CPU_THRM_SDA 51
DIODE1: CPU

SMC "A" SMBus Connections

NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE

6 =PP3V3_S3_SMBUS_SMC_A_S3

SMC
U4900
(MASTER)
45 SMB_A_S3_CLK
45 SMB_A_S3_DATA
88 SMBUS_SMC_A_S3_SCL
MAKE_BASE=TRUE
88 SMBUS_SMC_A_S3_SDA
MAKE_BASE=TRUE

R5270 4.7K 5% 1/16W MF-LF 402
R5271 4.7K 5% 1/16W MF-LF 402

ALS
(WRITE: 0X72 READ: 0X73)
TP_I2C_ALS_SCL
TP_I2C_ALS_SDA

POTENTIAL SMC SLAVE SMBUS CONNECTIONS

6 =PP3V3_S0_SMBUS_SMC_BSA

THIS CONNECTION IS BROKEN THROUGH NOSTUFF RESISTORS ON PAGE 90

SMC
U4900
(MASTER)
45 SMB_BSA_CLK
45 SMB_BSA_DATA
88 SMBUS_SMC_BSA_SCL
MAKE_BASE=TRUE
88 SMBUS_SMC_BSA_SDA
MAKE_BASE=TRUE

R5280 100K 5% 1/16W MF-LF 402
R5281 100K 5% 1/16W MF-LF 402

DISPLAY TCON
DP RX MASTER FOR MCCS
SMC SLAVE ADDRESS TBD
=SMB_DP_TCON_SCL 77
=SMB_DP_TCON_SDA 77

SMC "MANAGEMENT" SMBUS CONNECTIONS

6 =PP3V3_S0_SMBUS_SMC_MGMT

SMC
U4900
(MASTER)
45 SMB_MGMT_CLK
45 SMB_MGMT_DATA
88 SMBUS_SMC_MGMT_SCL
MAKE_BASE=TRUE
88 SMBUS_SMC_MGMT_SDA
MAKE_BASE=TRUE

R5290 4.7K 5% 1/16W MF-LF 402
R5291 4.7K 5% 1/16W MF-LF 402

DP RX EQLZ CONTROL
U9200
(WRITE: 0X92 READ: 0X93)
=I2C_DP_EQLZ_SCL 79
=I2C_DP_EQLZ_SDA 79

DP TX EQLZ CONTROL
U9100
(WRITE: 0X9C READ: 0X9D)
=I2C_DP_DRV_SCL 78
=I2C_DP_DRV_SDA 78

SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE
SMBus Connections

Apple Inc.

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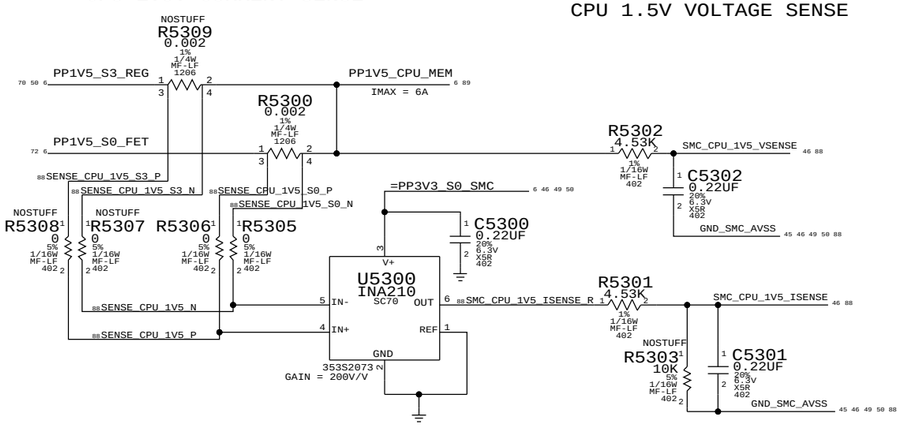
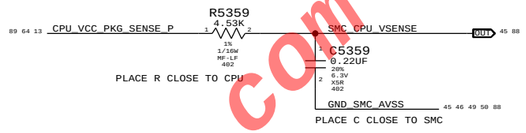
CPU 1.5V CURRENT SENSE

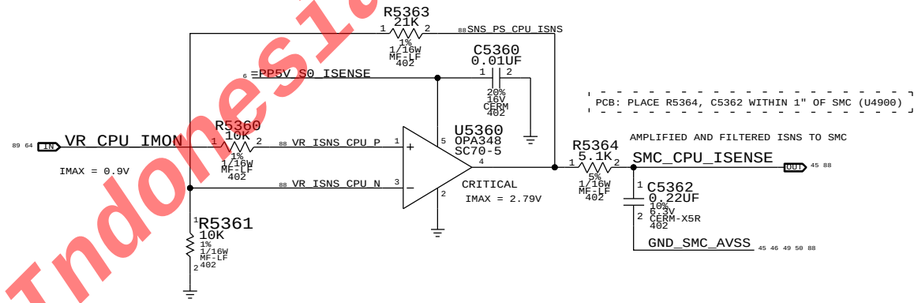


CPU 1.5V VOLTAGE SENSE

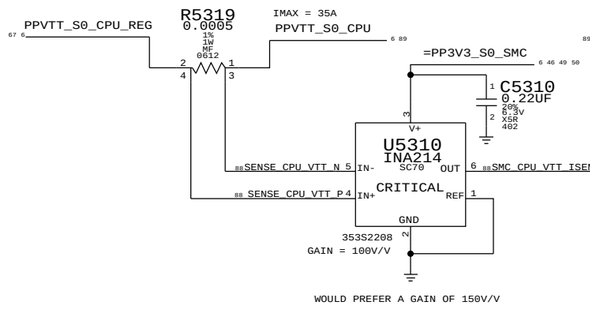
CPU Voltage Sense / Filter



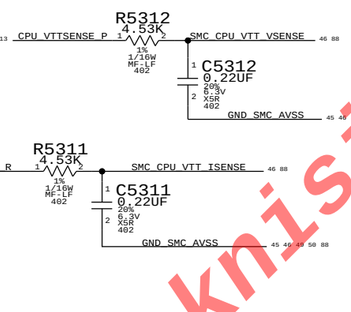
CPU CURRENT SENSE AMP & FILTER



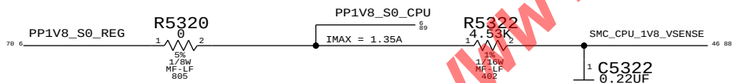
CPU VTT CURRENT SENSE



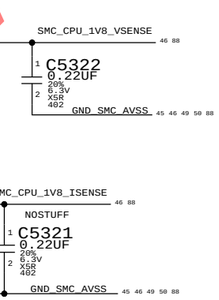
CPU VTT VOLTAGE SENSE



CPU 1.8V CURRENT SENSE



CPU 1.8V VOLTAGE SENSE



SYNC MASTER=K60_JERRY SYNC DATE=07/01/2009

PAGE TITLE

CPU POWER SENSE

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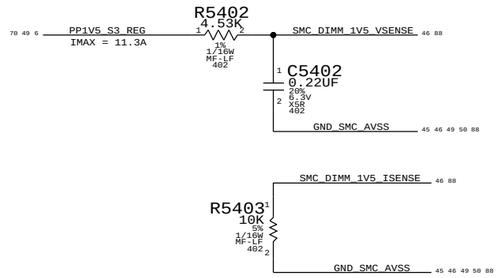
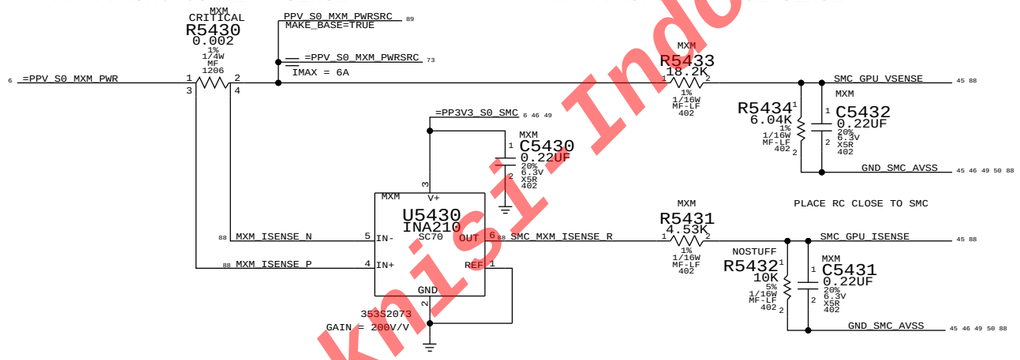
1.5V S3 VOLTAGE SENSE



MXM PWRSRC CURRENT SENSE

MXM PWRSRC VOLTAGE SENSE



SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE
GRAPHICS / DIMM POWER SENSE

Apple Inc.

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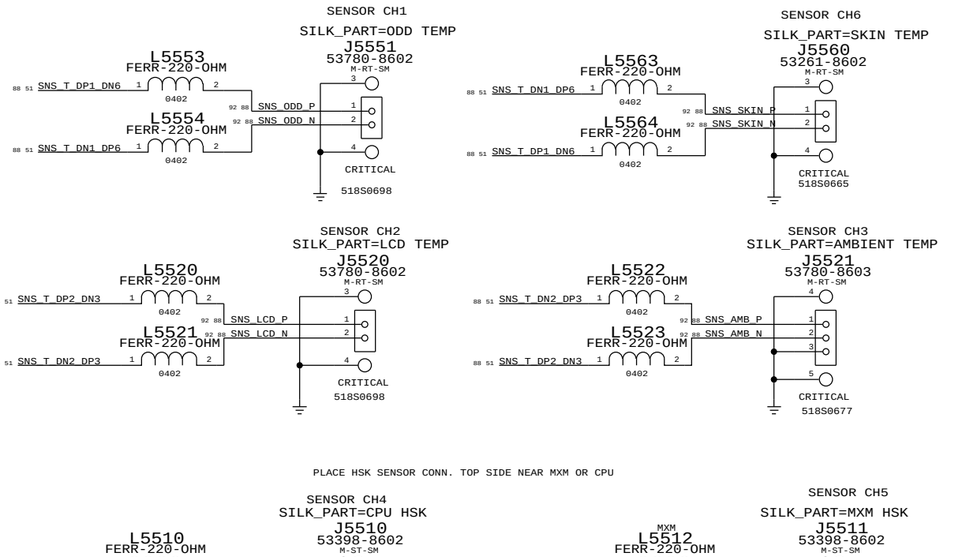
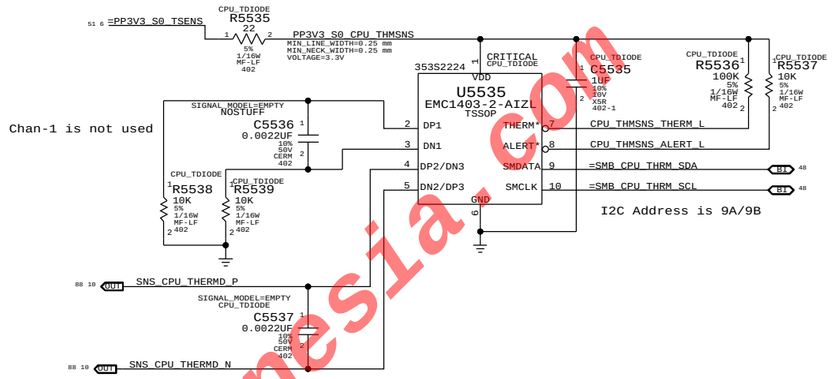
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

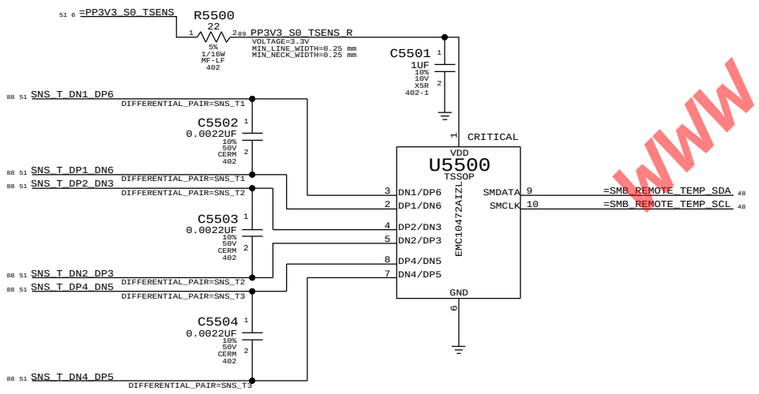
REMOTE THERMAL SENSORS
HEATSINKS, AMBIENT, PANEL AND ODD



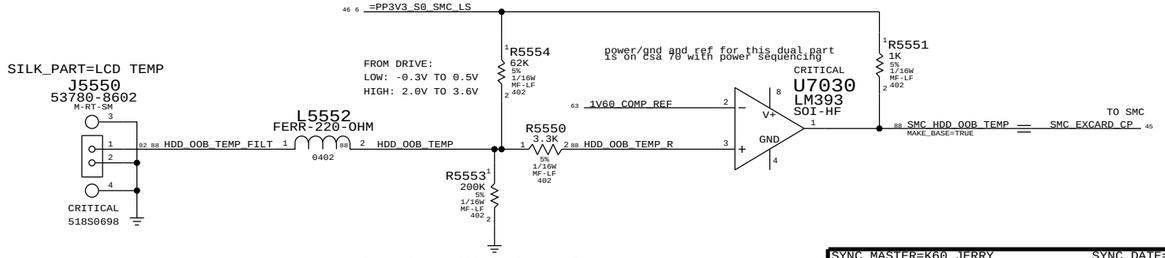
CPU T-DIODE THERMAL SENSOR



REMOTE THERMAL SENSORS (HEATSINKS AND ODD)



HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

PAGE TITLE: Thermal Sensors

Apple Inc.

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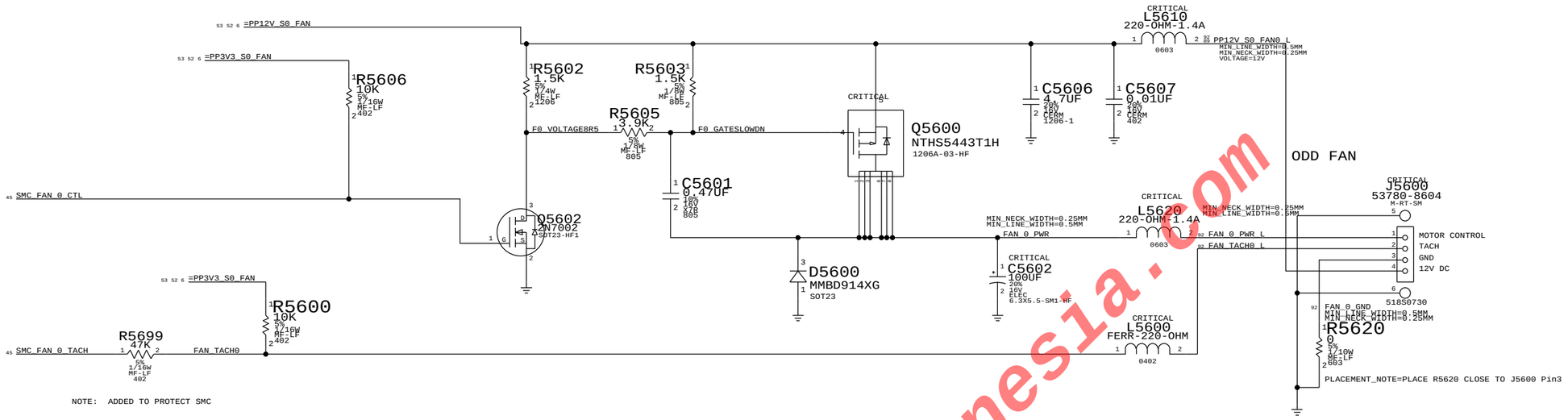
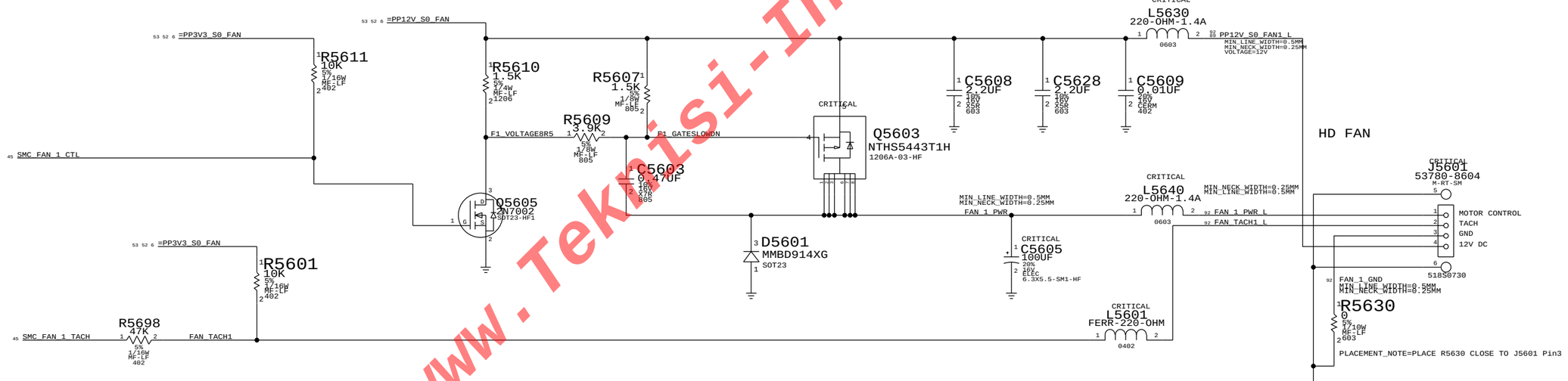
FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



SYNC_MASTER=K60_DEREK SYNC_DATE=07/01/2009

PAGE TITLE: HD AND OD FAN

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

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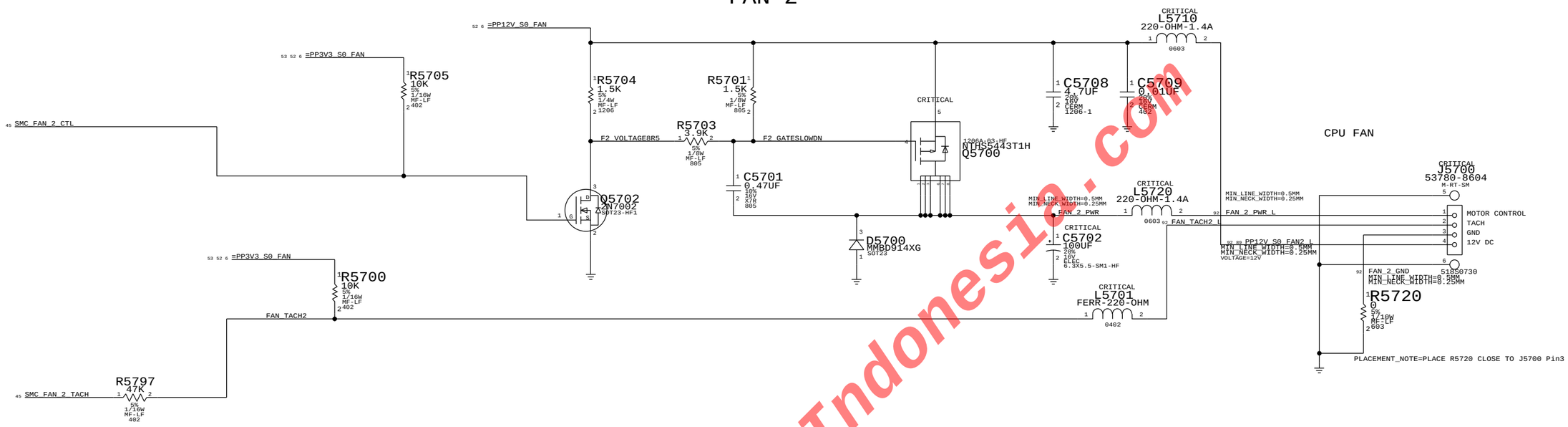
FAN 2



SYNC MASTER=K60_DEREK SYNC DATE=07/01/2009

PAGE TITLE: CPU FAN

Apple Inc.

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REVISION: B.0.0

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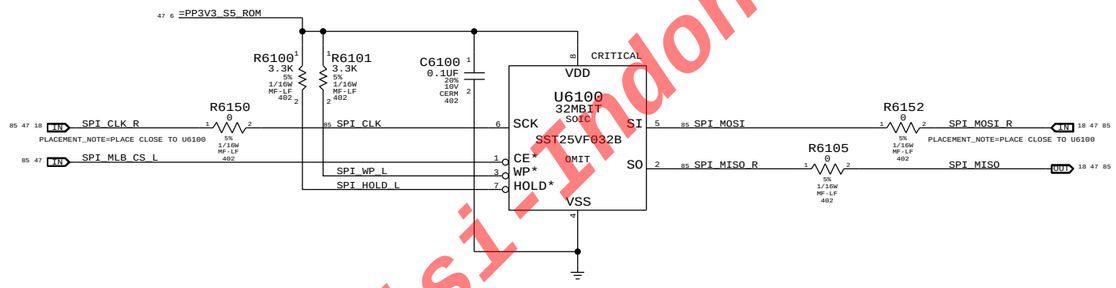

SYNC MASTER=K60 SIJI SYNC DATE=07/01/2009

PAGE TITLE

SPI ROM

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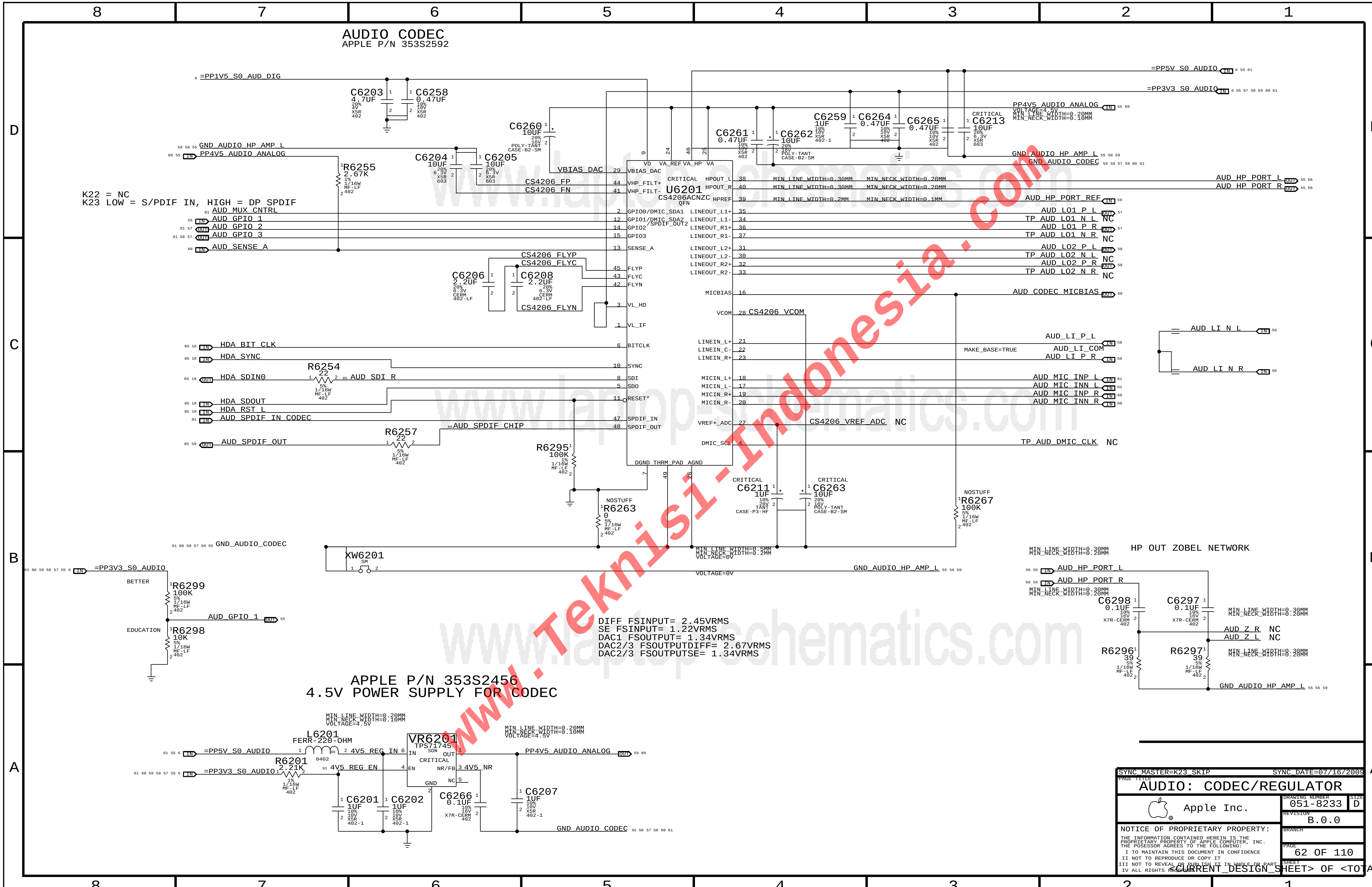

SYNC_MASTER=K23_SKIP SYNC_DATE=07/16/2009

PAGE TITLE

AUDIO: CODEC/REGULATOR

Apple Inc.

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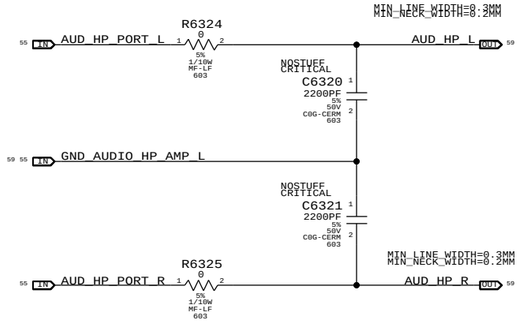
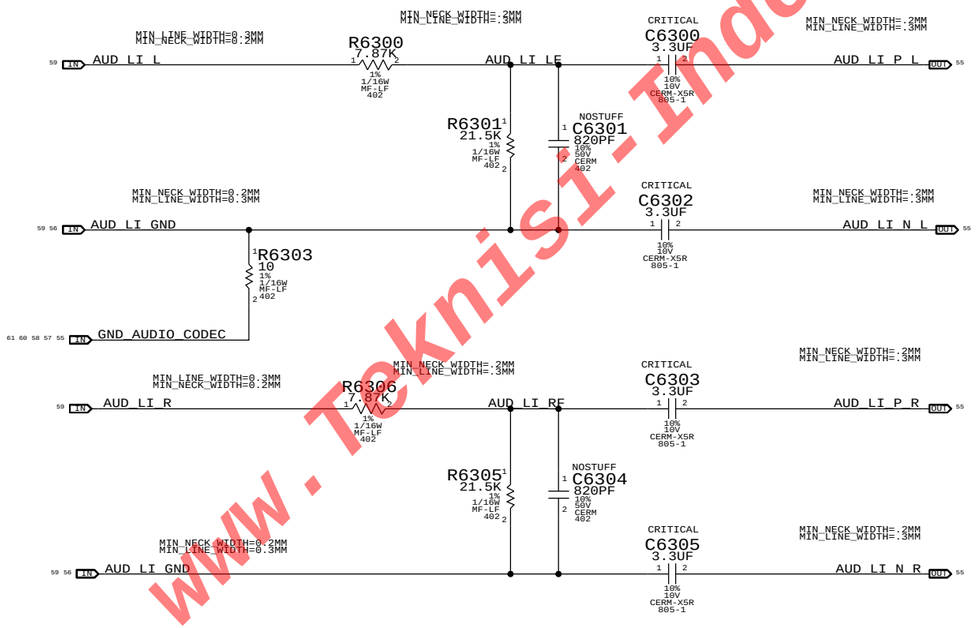
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

1ST ORDER DAC FILTER PLACEHOLDER



CODEC_Nom SE RIN = 20K OHMS
FC = 5 HZ Max
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



SYNC_MASTER=K23_SKIP SYNC_DATE=07/16/2009

PAGE TITLE
AUDIO: FILTER/BUFFER

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION B.0.0
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PAGE 63 OF 110
SHEET

<CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

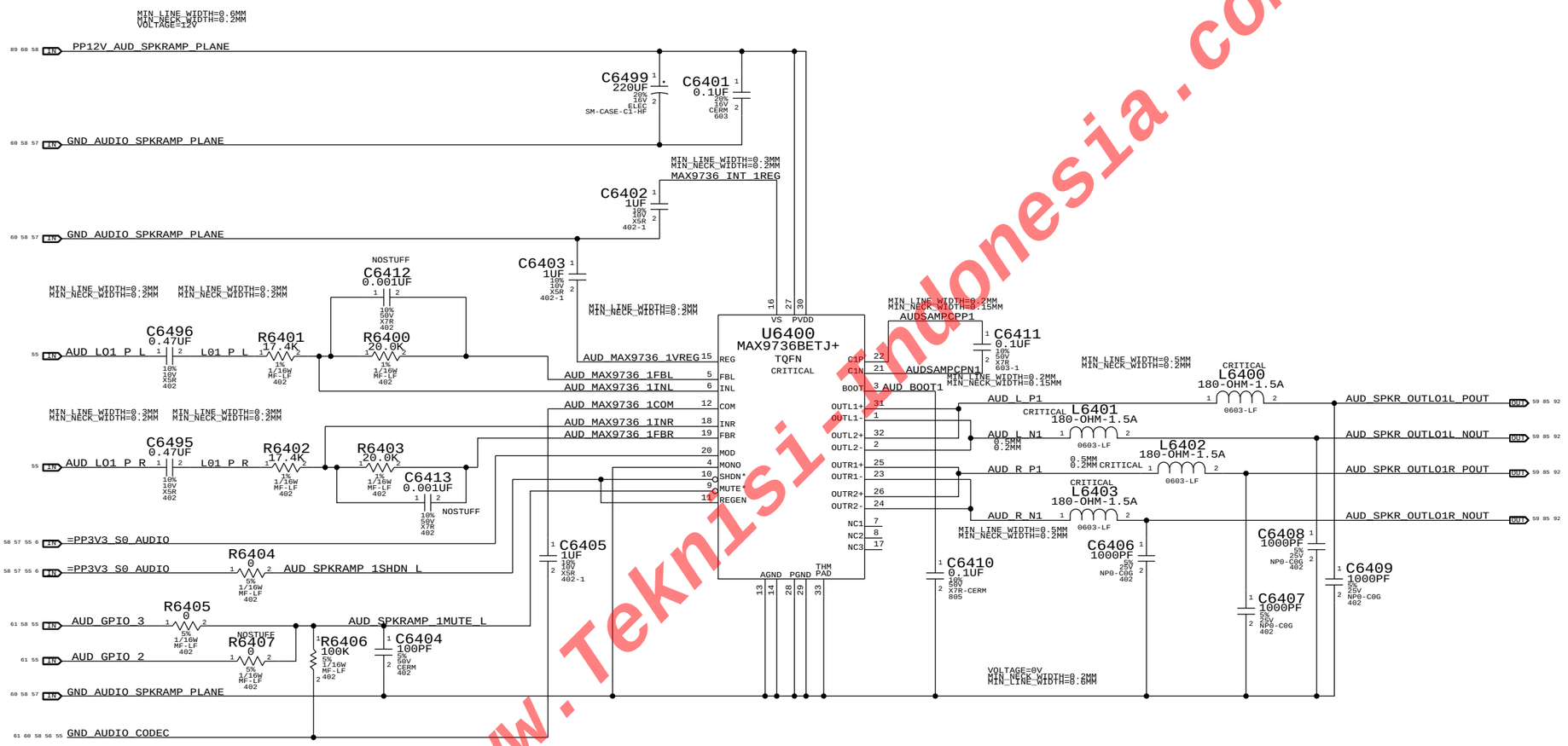
TWEETER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ

POUT = 6.76 W INTO 8 OHMS @ 1% THD+N



SYNC_MASTER=K23_SKIP SYNC_DATE=07/16/2009

PAGE TITLE: AUDIO: Tweeter Amp 1

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

REVISION: B.0.0

BRANCH:

PAGE: 64 OF 110

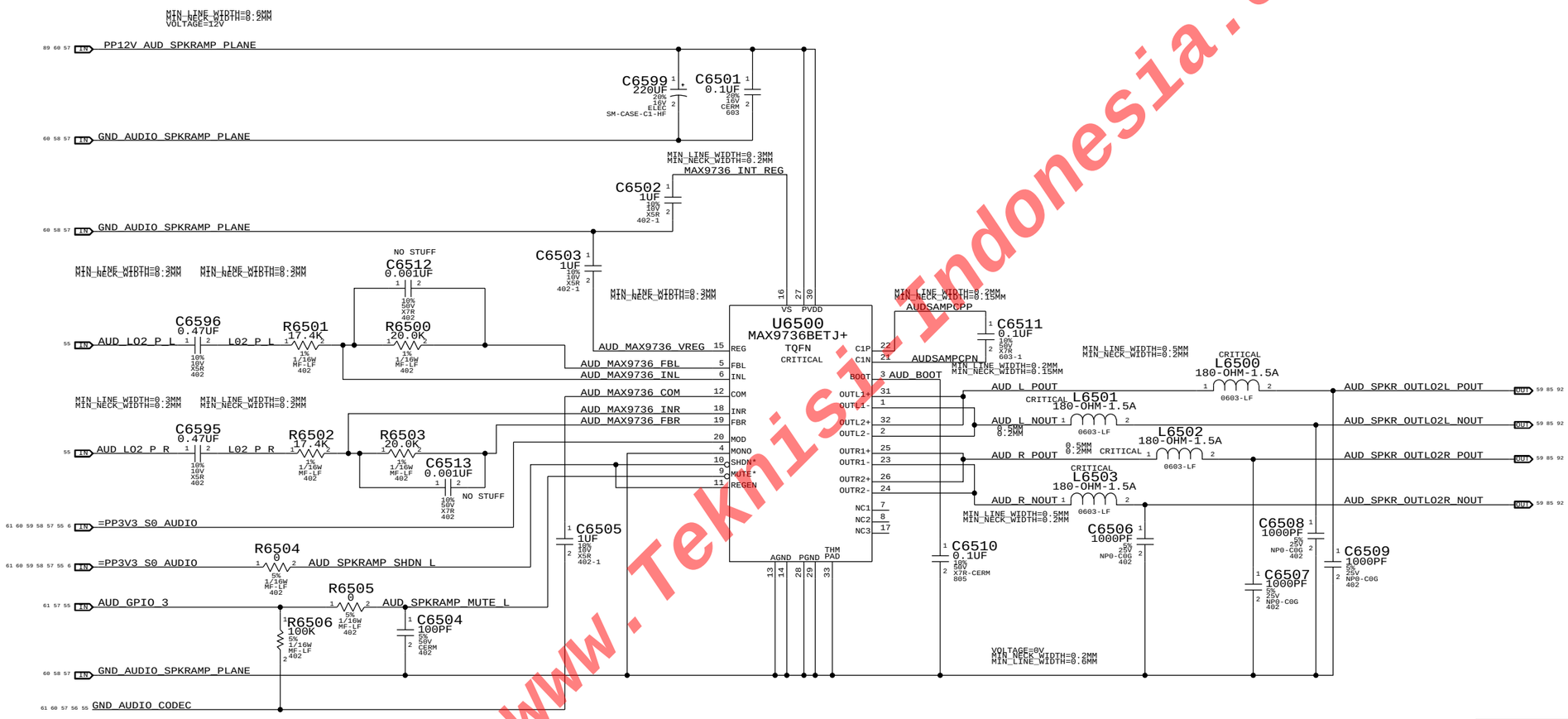
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

WOOFER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ



SYNC_MASTER=K23_SKIP SYNC_DATE=07/16/2009

PAGE TITLE: AUDIO: Woofer Amp

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D
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PAGE: 65 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

INTERNAL MIC CON
APPLE P/N 518S0677

SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656

REMOTE I/O CONNECTOR
APPLE P/N 518S0723

SYNC_MASTER=K60	SYNC_DATE=06/05/2009
PAGE TITLE	Audio: MLB to I/O Conn.
Apple Inc.	DRAWING NUMBER 051-8233 SIZE D
	REVISION B.0.0
	BRANCH
	PAGE 66 OF 110
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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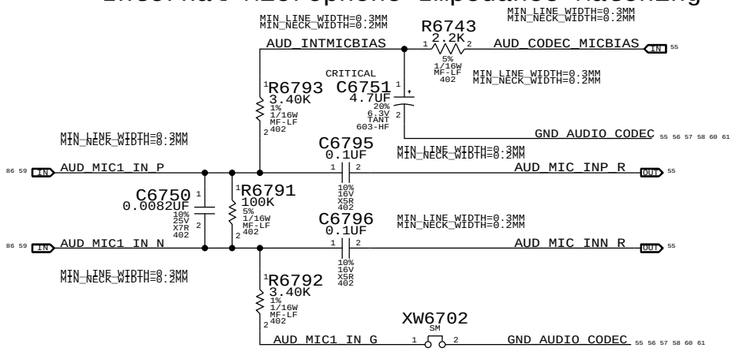
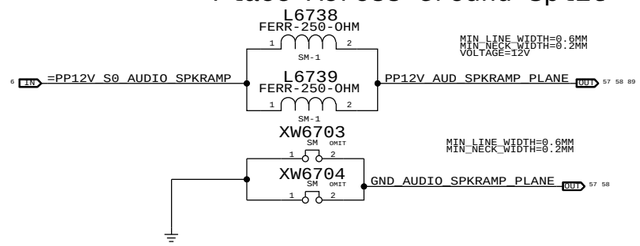
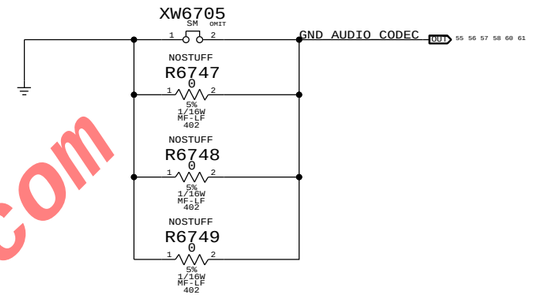
Internal Microphone Impedance Matching



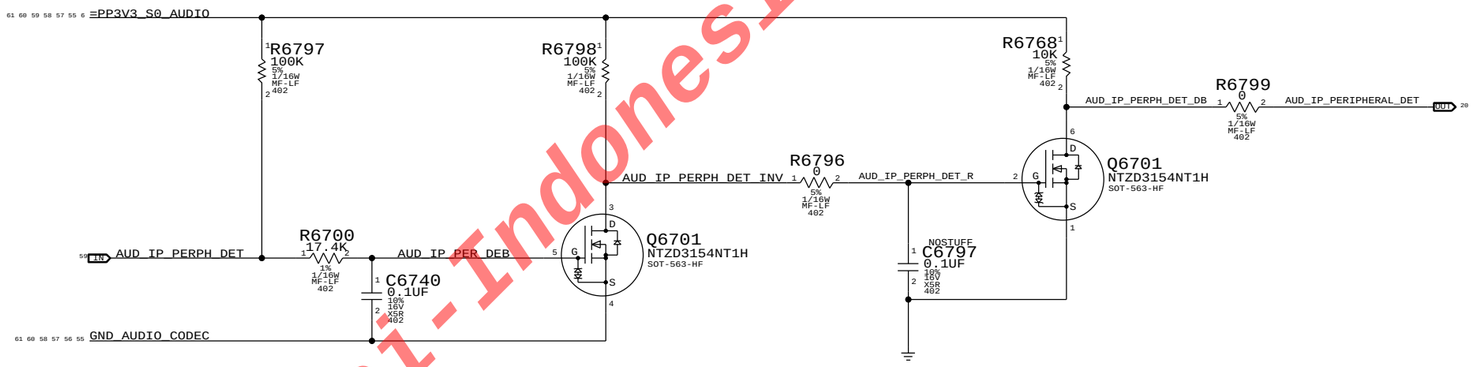
Place Across Ground Split



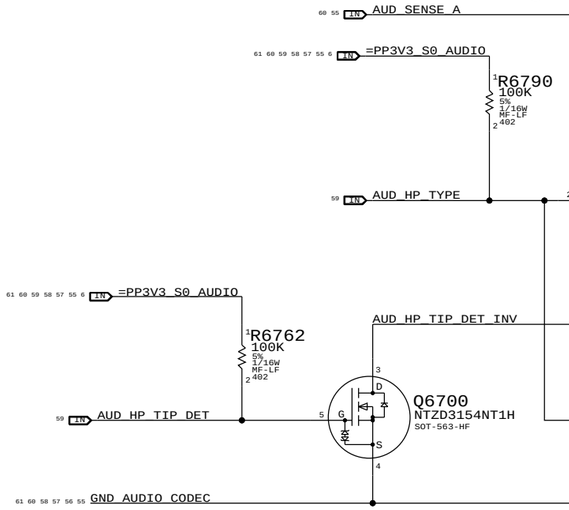
Audio Ground Returns



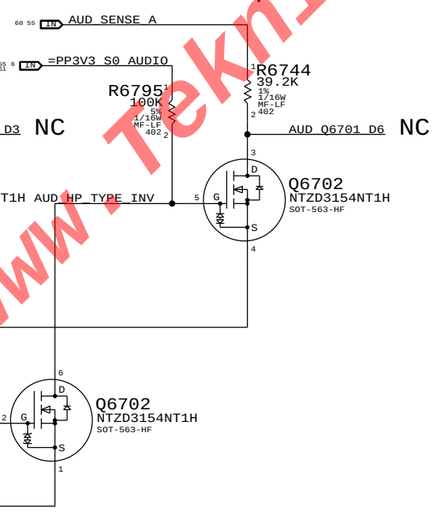
IPHS HS Detect Debounce CKT



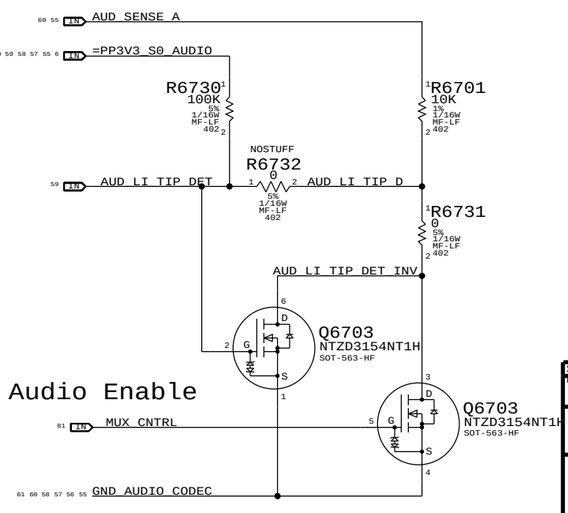
Digital Out



Headphone Out



LI Insert Detect



DP Audio Enable

SYNC_MASTER=K23_SKIP SYNC_DATE=07/16/2009

PAGE_TITLE: AUDIO: Detects/Grounding

Apple Inc.

DRAWING_NUMBER: 051-8233 SIZE: D

REVISION: B.0.0

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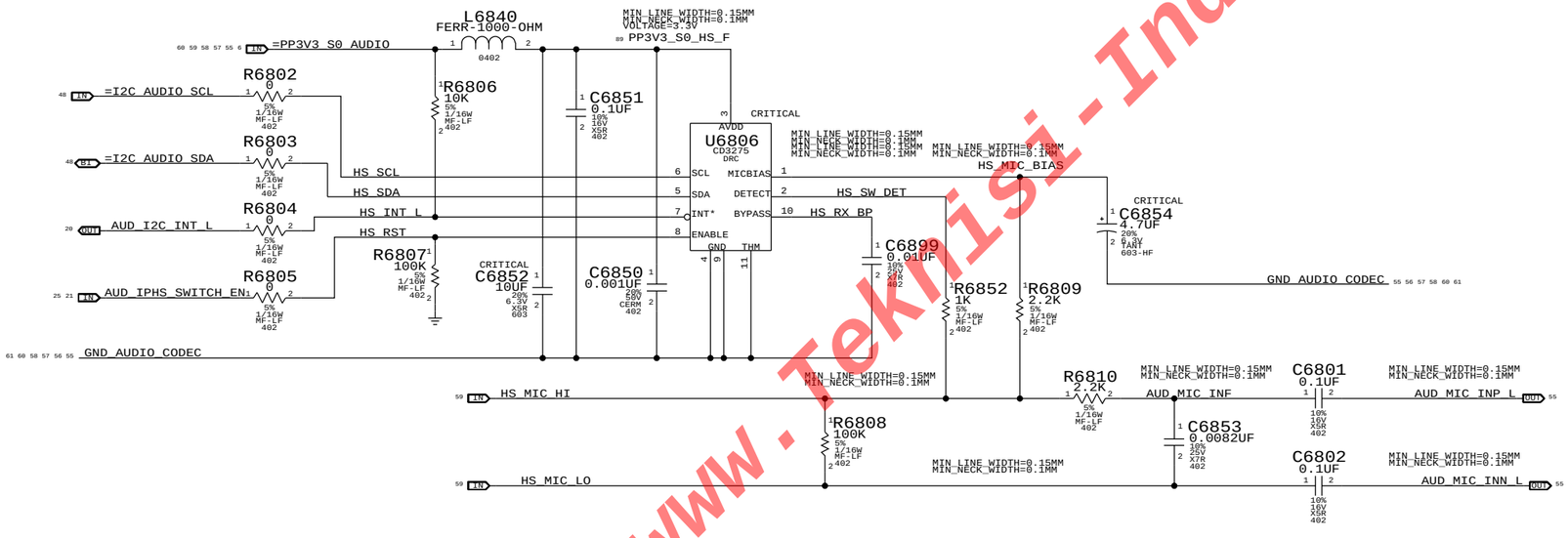
PAGE: 67 OF 110

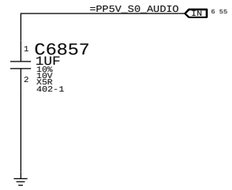
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

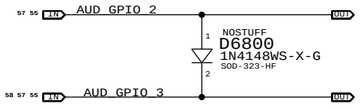
FUNCTION	PIN	CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/INTERRUPT
PRIMARY	0X0B	0X04	0X04	GPIO 3	N/A
SECONDARY	0X0A	0X03	0X03	GPIO 3	N/A
HEADPHONES	0X09	0X02	0X02	N/A	0X09 (A)
LINE INPUT	0X0C	0X05	0X05	N/A	LINE IN
BUILT-IN MICROPHONE	0X0D(13,B,RIGHT)	0X06	0X06	MICBIAS 80%	N/A
HEADSET MICROPHONE	0X0D (13,V22,B,LEFT)	0X06	0X06	MIKEY	MIKEY
SPDIF OUT	0X10	0X08	N/A	N/A	0X0C (B)
SPDIF IN	0X0F	0X07	N/A	N/A	N/A
MIKEY	N/A	N/A	N/A	MCP GPIO_38	MCP GPIO_5

MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256







FLP = 8.82 KHZ
FHP = 80 HZ

SYNC MASTER=K23 SKIP SYNC DATE=07/16/2009

PAGE TITLE: AUDIO: Mikey

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

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SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

SLP_S4 ENABLES

State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

R6901 0 5% 1/16W MF-LF 402
91 48 PM_RSMRST_L IN 1 — 2 PM_RSMRST_PCH_L OUT 19 91

MEMVTT_EN SEQUENCE

72 63 62 6 5 =PP3V3_S0_PWRCTL
R6951 10K 5% 1/16W MF-LF 402
R6952 10K 5% 1/16W MF-LF 402
R6953 0 5% 1/16W MF-LF 402
DDRVTT_EN 32 62 70 91
NOSTUFF C6951 100PF 5% 50V CERM 402
VTT_REG_PGOOD_R2
VTT_REG_PGOOD_R1
Q6911 MMDT3904-X-G SOT-363-LF
NOSTUFF C6953 0.1UF 10% 10V X5R 402
67 63 62 11 91 CPUVTT_REG_PGOOD
R6950 100K 5% 1/16W MF-LF 402
Q6911 MMDT3904-X-G SOT-363-LF
NOSTUFF C6952 0.47UF 10% 6.3V CERM-X5R 402

63 62 6 5 =PP3V3_S5_PWRCTL
C6910 0.1UF 20% 10V CERM 402
91 19 PM_SLP_S4_1_L
U6900 08 74LVC08 TSSOP-HF
S4_ENABLES
63 62 6 5 =PP3V3_S5_PWRCTL
R6916 100K 5% 1/16W MF-LF 402
R6915 10K 5% 1/16W MF-LF 402
CPU_SKTOCC
Q6910 2N7002DW-X-G SOT-363
11 CPU_SKTOCC_L
NOSTUFF R6917 0 5% 1/16W MF-LF 402

PLACE TOP SIDE
REWORK TO POWER UP WITH NO CPU

R6911 33 5% 1/16W MF-LF 402
P3V3S3_EN 72 91 Enable FET
R6912 33 5% 1/16W MF-LF 402
P5VS3_EN 69 91 ENABLE REGULATOR
R6914 33 5% 1/16W MF-LF 402
P12V_S3_EN 72 91 Enable FET
NOSTUFF C6920 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6921 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6923 0.47UF 10% 6.3V CERM-X5R 402

6 =PP5V_S3_PWRCTL
R6910 100K 5% 1/16W MF-LF 402
69 P5VS3_REG_PGOOD MAKE_BASE=TRUE
PM_EN_USB_PWR 43
NOSTUFF C6924 0.47UF 10% 6.3V CERM-X5R 402
=DDRREG_EN 70

SLP_M ENABLES

THIS SLP_M CIRCUIT IS A BACKUP IN CASE
VCC_ME IS REQUIRED IN ANY STATE
OTHER THAN S0. DELETE AFTER PROTO1

NOSTUFF R6920 33 5% 1/16W MF-LF 402
Enable FET
P3V3ME_EN 72 91
PLACE SERIES R'S NEAR SOURCE

91 19 5 PM_SLP_M_L
R6922 1K 5% 1/16W MF-LF 402
P1V05_ME_SM_EN 72 91 Enable FET
R6927 0 5% 1/16W MF-LF 402
72 63 62 6 5 =PP3V3_S0_PWRCTL
=PP3V3_S5_PWRCTL
C6925 1UF 10% 6.3V CERM 402
P1V05_SM_DIS_L
62 PM_SLP_S3_BUF_L
R6925 10K 5% 1/16W MF-LF 402
PM_SLP_S3_B_R
74LVC08 TSSOP-HF
U6900 08
P1V05_ME_SM_DIS
Q6910 2N7002DW-X-G SOT-363
PCHCORE_PGOOD_R
68 63 62 5 91 PCHCORE_REG_PGOOD
R6926 10K 5% 1/16W MF-LF 402
C6926 1UF 10% 6.3V CERM 402

SLP_S3 ENABLES

63 62 6 5 =PP3V3_S5_PWRCTL
91 63 46 37 33 32 19 5 PM_SLP_S3_L
74LVC08 TSSOP-HF
U6900 08
(PM_SLP_S3_L_BUF)
MAKE_BASE=TRUE
63 PGOOD_P12V_S0
R6944 10K 1% 1/16W MF-LF 402
NOSTUFF R6941 10K 5% 1/16W MF-LF 402
91 70 5 PM_PGOOD_DDRREG_S3
R6948 0 5% 1/16W MF-LF 402
switch to alias after proto1
NOSTUFF C6947 0.47UF 10% 6.3V CERM-X5R 402

R6946 33 5% 1/16W MF-LF 402
P3V3S0_EN Enable FET 72 91
R6947 33 5% 1/16W MF-LF 402
P5VS0_EN Enable FET 72 91
PM_SLP_S3_BUF_L 62
Enable FET
P1V5_S0_EN 72 91
DDRVTT_EN 92 62 70 91 Enable regulator
NOSTUFF C6944 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6941 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6945 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C6946 0.47UF 10% 6.3V CERM-X5R 402

OTHER RAILS ENABLED BY P3V3_S0 AND P5V_S0:
PP1V8_S0 VREG (CPU PLL)

72 63 62 6 5 =PP3V3_S0_PWRCTL
R6942 10K 5% 1/16W MF-LF 402
Enable regulator
PCHCORE_REG_EN
PCHCORE VREG
68 91 91 68 63 62 5
PCHCORE_REG_PGOOD
MAKE_BASE=TRUE
ENABLE FET
P1V05_ME_S0_EN 72
91 72 PGOOD_P5V_S0
MAKE_BASE=TRUE
C6942 1UF 10% 6.3V CERM 402
R6949 0 5% 1/16W MF-LF 402
Enable regulator
CPUVTT_REG_EN
CPUVTT VREG
67 91 91 67 63 62 11
CPUVTT_REG_PGOOD
MAKE_BASE=TRUE
Enable regulator
PM_EN_PVCORE_CPU 64
TO ENABLE OF CPU VREG
switch to alias after proto1

SYNC_MASTER=K60_MIKE SYNC_DATE=07/07/2009
PAGE TITLE
POWER SEQUENCING ENABLES
Apple Inc.
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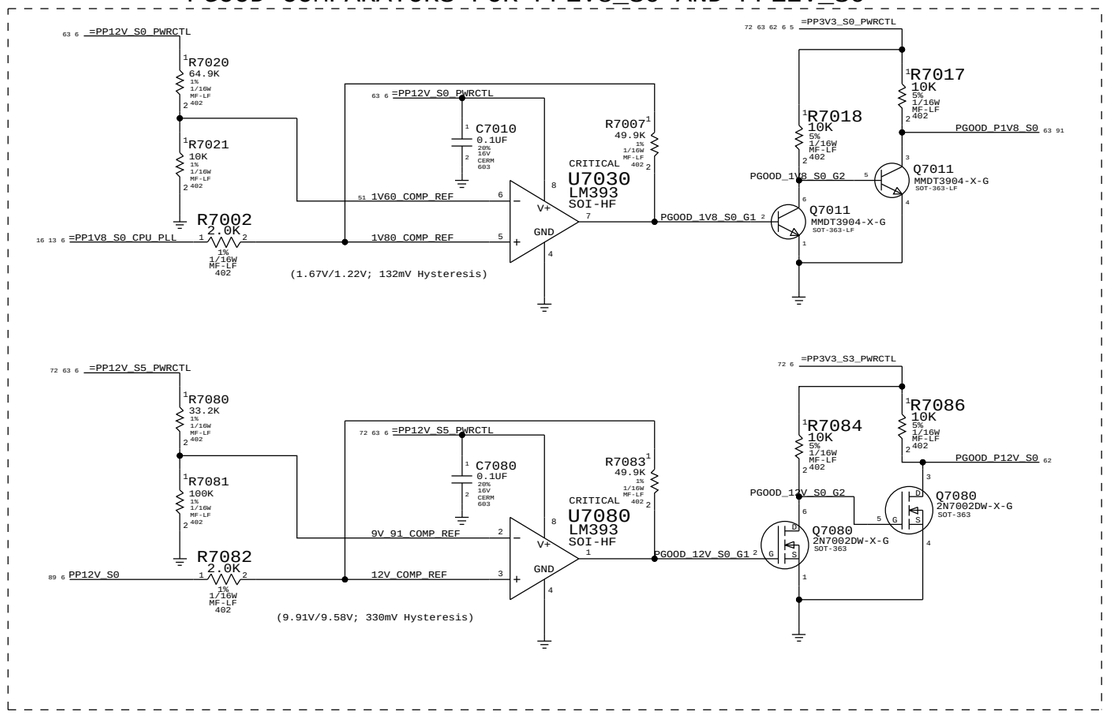
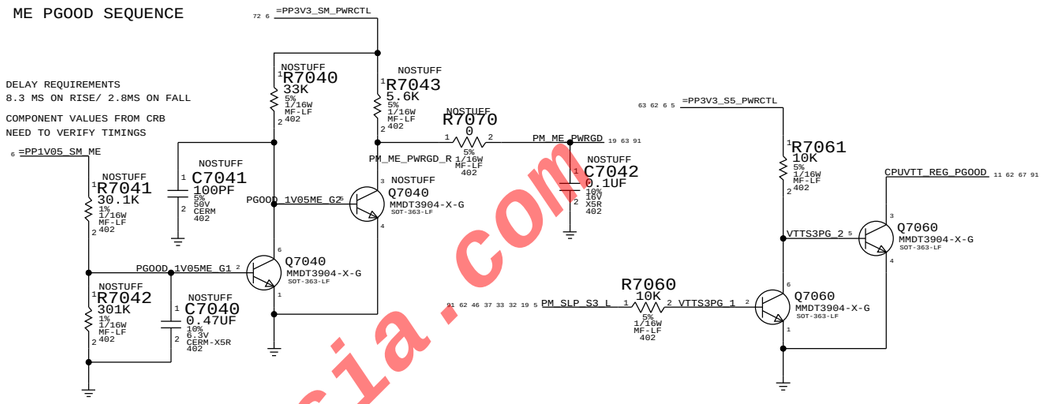
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PGOOD COMPARATORS FOR PP1V8_S0 AND PP12V_S0

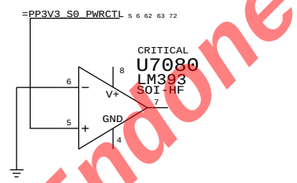


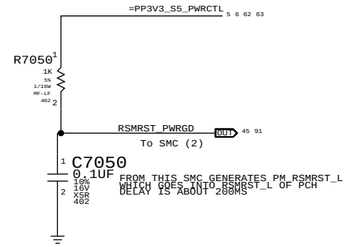
S0 RAILS PGOOD

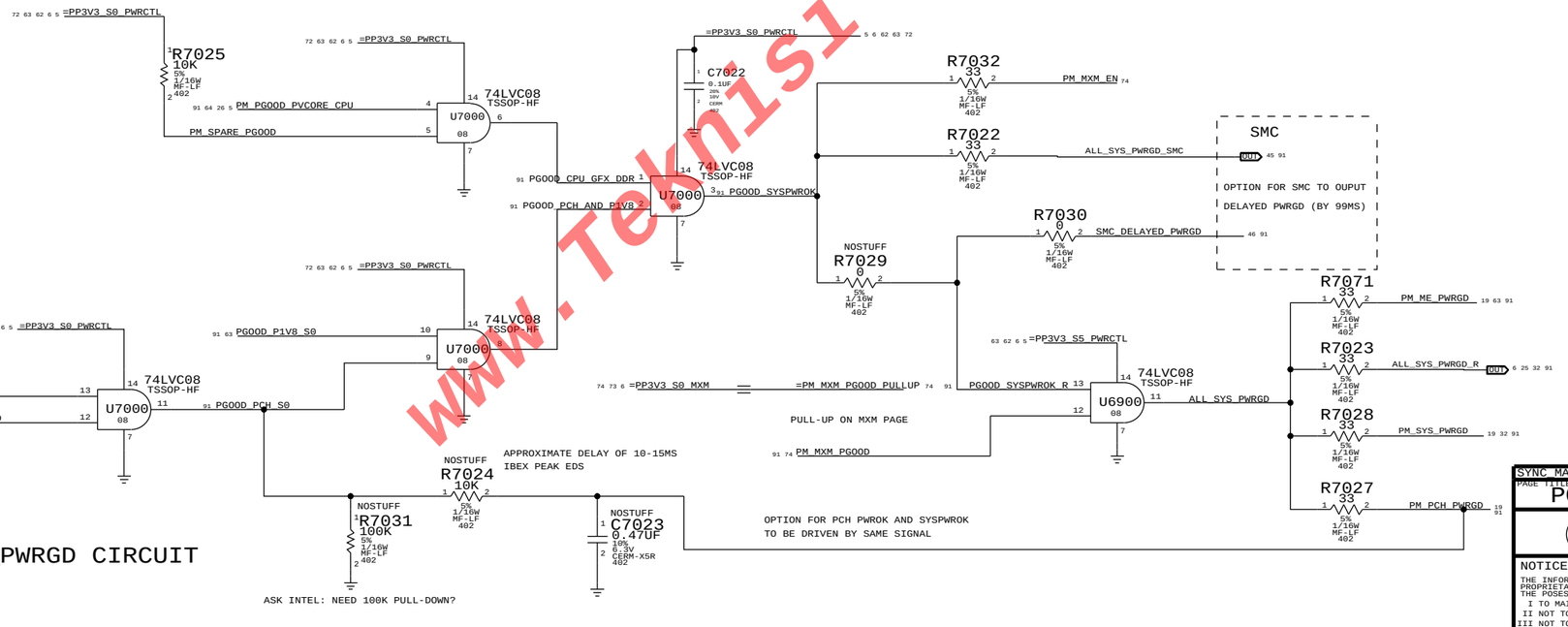
ME PGOOD SEQUENCE



DISABLE CPUVTT_REG_PGOOD WHEN SLP_S3_L = 0 (PER PIKETON PDG)







ALL_SYS_PWRGD CIRCUIT

SYNC_MASTER=K60_MIKE SYNC_DATE=07/01/2009

PAGE TITLE: POWER SEQUENCING PGOOD

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

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SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CPU CORE REG 1.1V/110A O/P= PPVCORE_S0_CPU_REG

CPU VCORE
VOUT = VCORE
PEAK = 110A
AVG = 90A

=PP5V_S0_VRD
PPVCORE_S0_CPU_REG
CPU_VCC_PKG_SENSE_P
CPU_VCC_PKG_SENSE_N
PP5V_S0_CPU_VCORE_VCC
PP5V_S0_CPU_VCORE_VCC
=PP3V3_S0_VRD
=PPVTT_S0_CPU
PM_EN_PVCORE_CPU
PM_PGOOD_PVCORE_CPU
VR_CPU_IOUT
CPU_PSI_L
CPU_VID<7..0>
=PP12V_S0_VRD
IMAX = 10.5A
PP12V_S0_CPU_FLTRD
LOCAL 5V
AGND_CPU
VR_CPU_PSI_L
VR_CPU_PWM1
VR_CPU_PWM2
VR_CPU_PWM3
VR_CPU_PWM4
VR_CPU_ISNS1_P
VR_CPU_ISNS1_N
VR_CPU_ISNS2_P
VR_CPU_ISNS2_N
VR_CPU_ISNS3_P
VR_CPU_ISNS3_N
VR_CPU_ISNS4_P
VR_CPU_ISNS4_N

MAX_NECK_LENGTH=3MM
MIN_NECK_WIDTH=0.3MM
MIN_LINE_WIDTH=0.8MM
VOLTAGE=5V

1.25 mOhm loadline

VR_HOT goes HIGH when VTM/VCC < 28% and LOW when VTM/VCC > 33%.

LAYOUT: PLACE RT7101 NEAR HOT SPOT.

U7100 ISL6334

CRITICAL L7100 0.36UH-45A-0.76MOHM MSQ1211R36LF-TH 152-0104

CPU CORE INPUT Filtering

SYNC_MASTER=K61_JERRY SYNC_DATE=07/16/2009

PAGE TITLE: VREG: PPVCORE_S0_CPU

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DRAWING NUMBER: 051-8233 SIZE: D
REVISION: B.0.0
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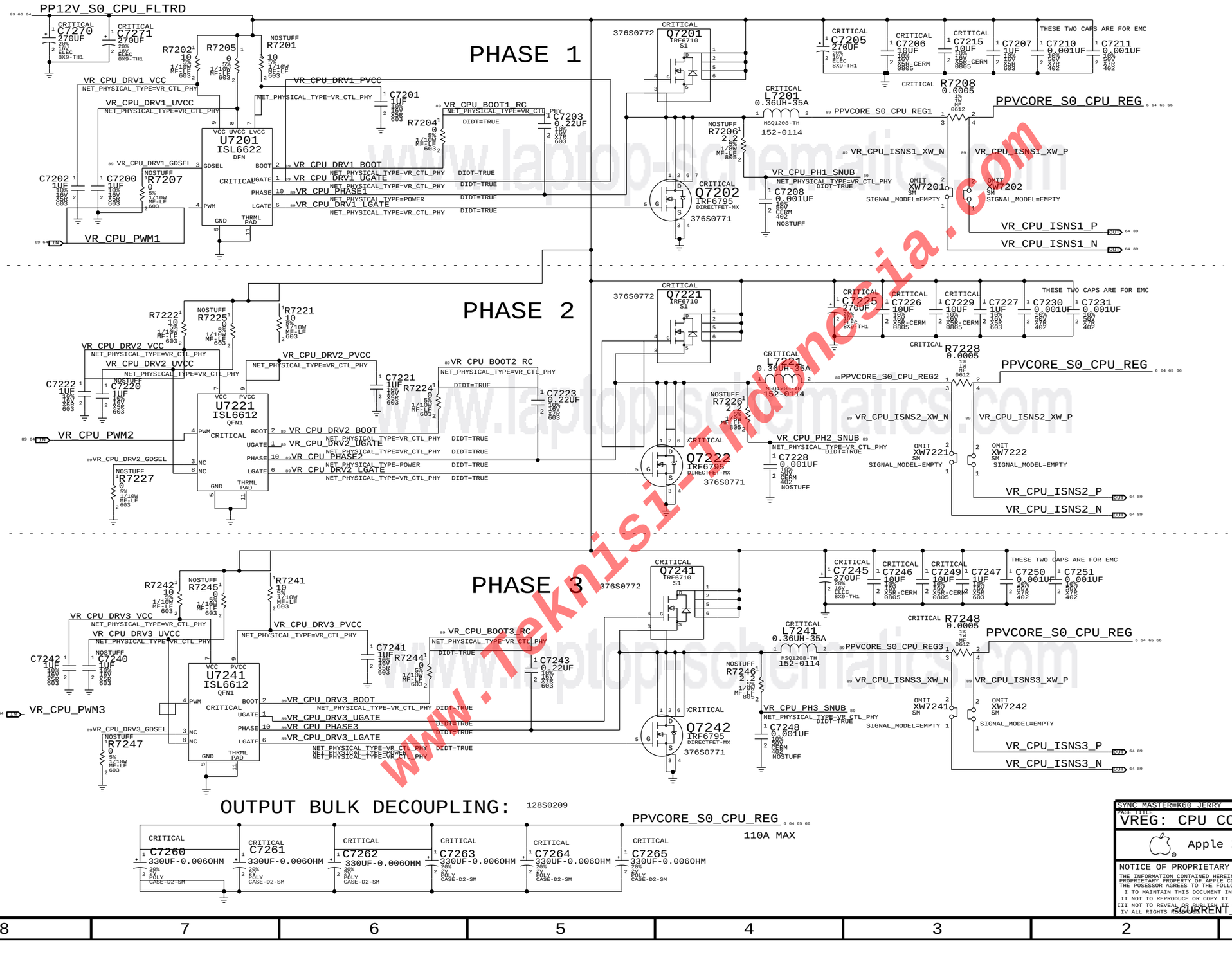
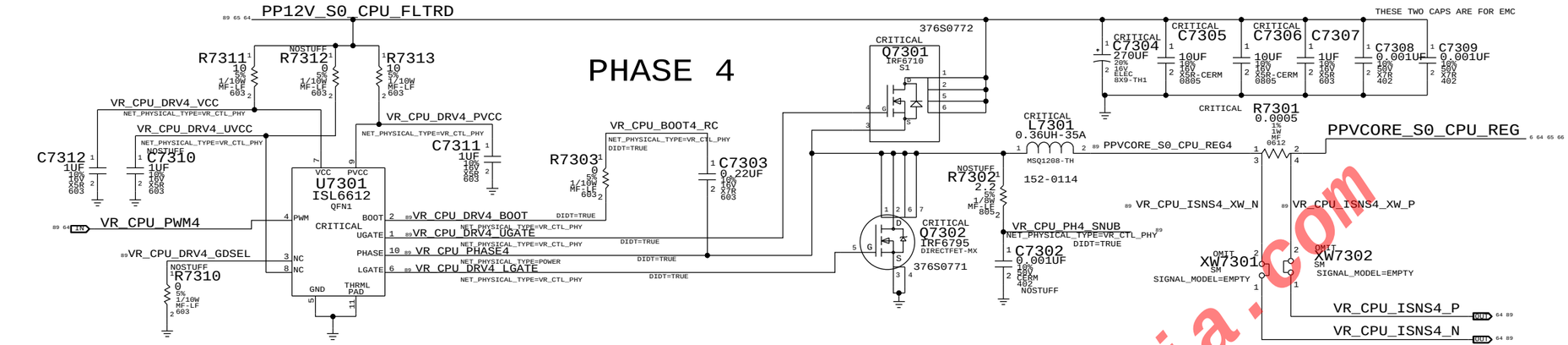
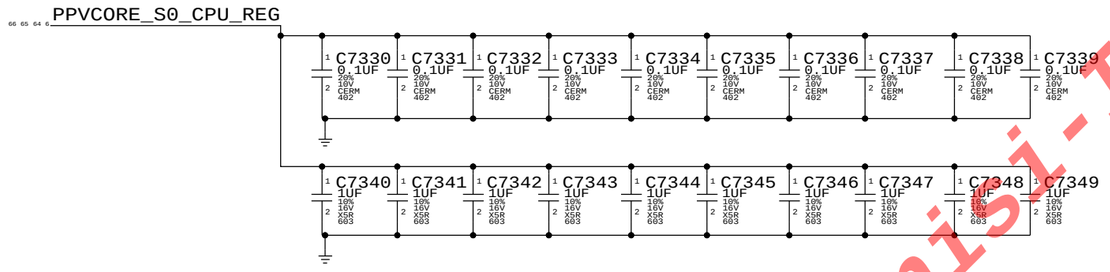
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



PHASE 4





SYNC MASTER=K61 JERRY SYNC DATE=07/16/2009

PAGE TITLE: VREG: CPU CORE - PHASE 4

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

REVISION: B.0.0

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PAGE: 73 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CPU VTT REG 1.1V/30A O/P= PPVTT_S0_CPU_REG

CPU VTT
VOUT = 1.1V OR 1.05V
PEAK = 35A
AVG = 30A

=PP12V_S0_CPU_VTT_VREG
=PP5V_S0_CPU_VTT_VREG
CPUVTT_REG_PGOOD "PULL-UP" TO VTT RAIL ON CPU PAGE
CPUVTT_REG_EN
PP5V_CPUVTT_VR
PPVTT_S0_CPU_REG

VID0=0, VID[4-1]=1, VTT VR o/p= 1.10V
Internal Pu on VID lines

(SELECT MODE= VRM10)

U7400 ISL6568 QFN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
113S0127	1	RES,68k,0603,5%	TH7401	

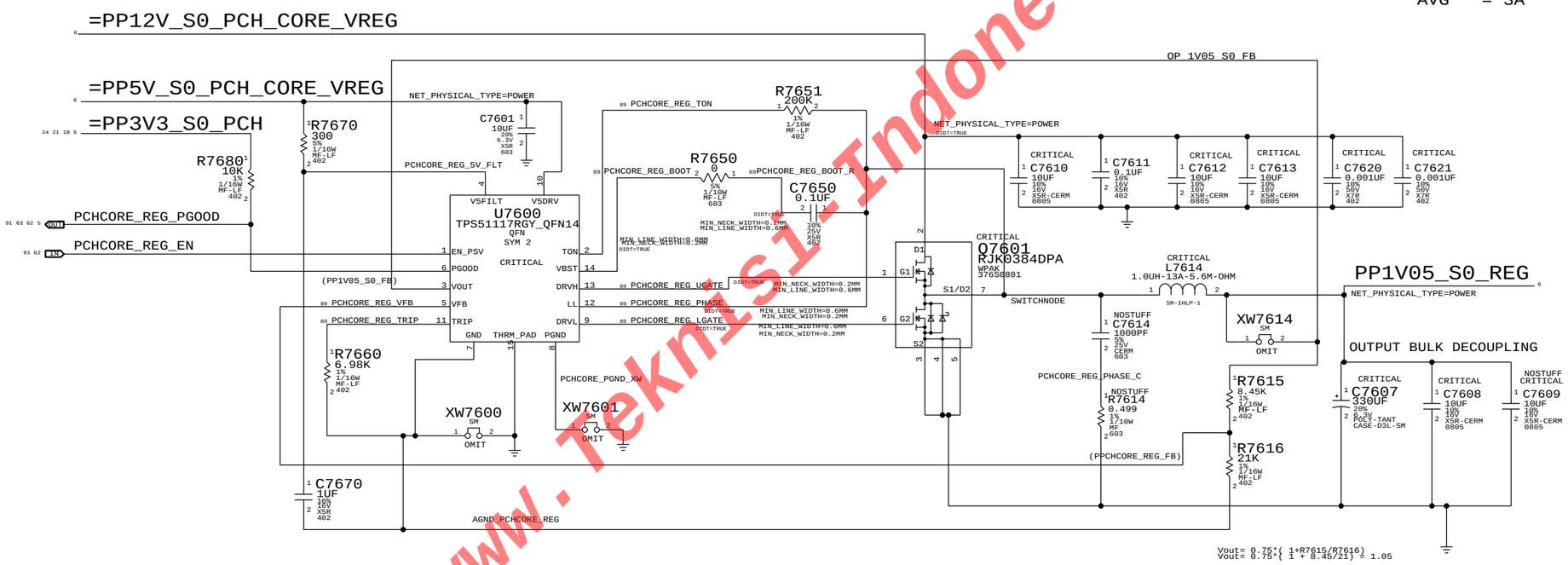
SYNC MASTER=K61 JERRY SYNC_DATE=07/16/2009
PAGE TITLE: CPU VTT REGULATOR

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D
REVISION: B.0.0
BRANCH:
PAGE: 74 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

IBEX PEAK CORE REG 1.05V OUTPUT = PP1V05_S0_REG

PP1V05_S0_REG
VOUT = 1.05V
PEAK = 7.5A
AVG = 3A



PAGE TITLE
IBEX PEAK CORE

Apple Inc.

DRAWING NUMBER 051-8233
SIZE D
REVISION B.0.0
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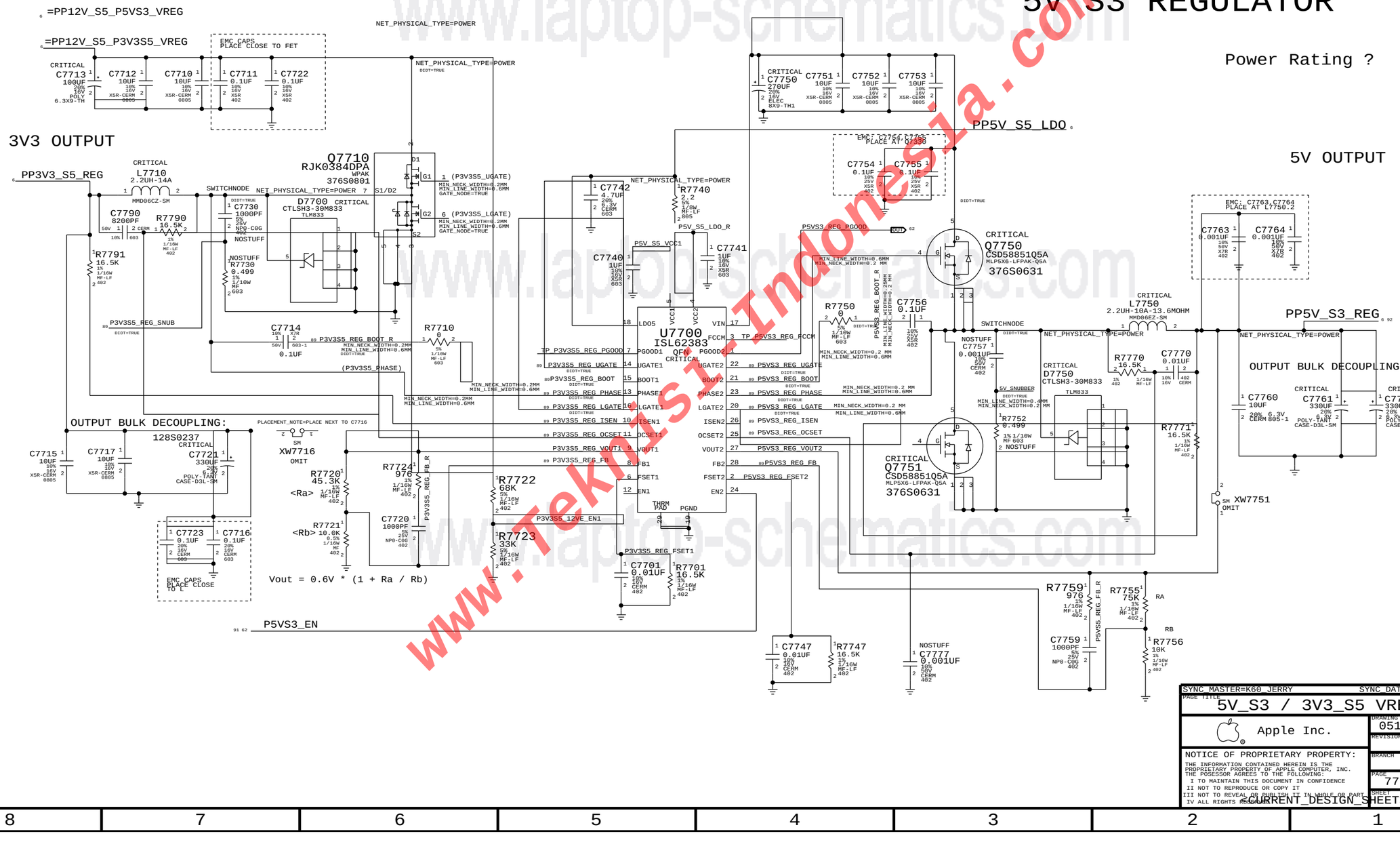
PAGE 76 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

3V3 S5 REGULATOR

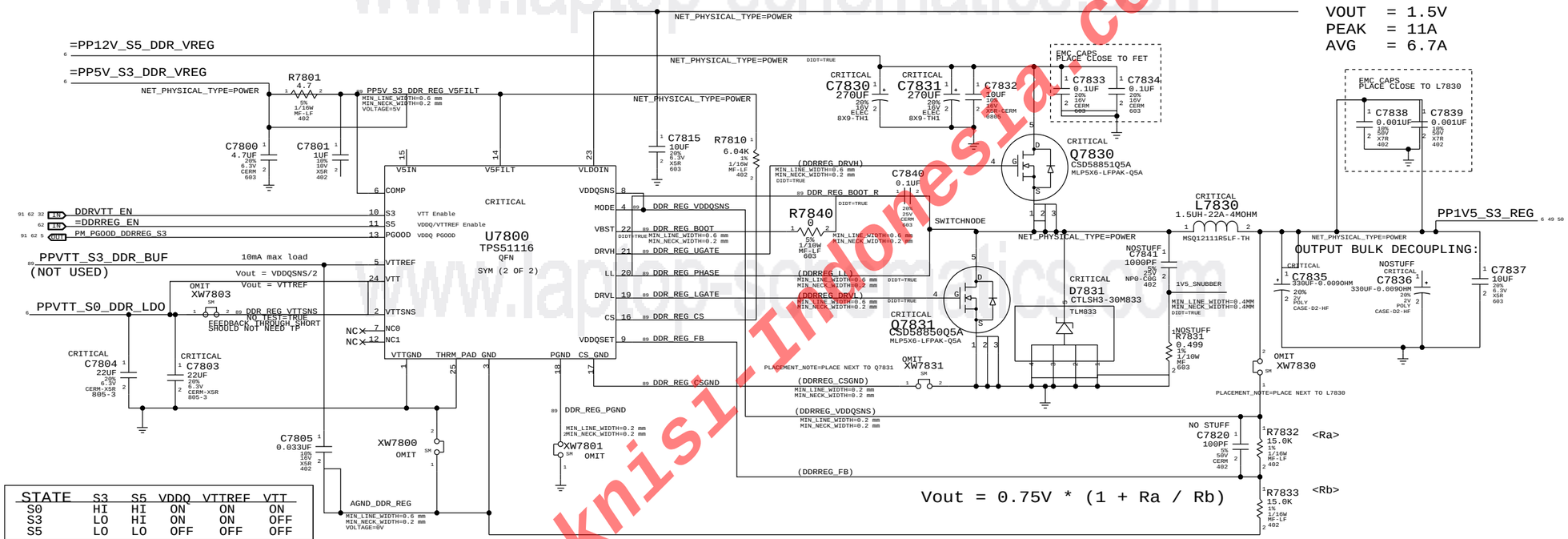
5V S3 REGULATOR

Power Rating ?

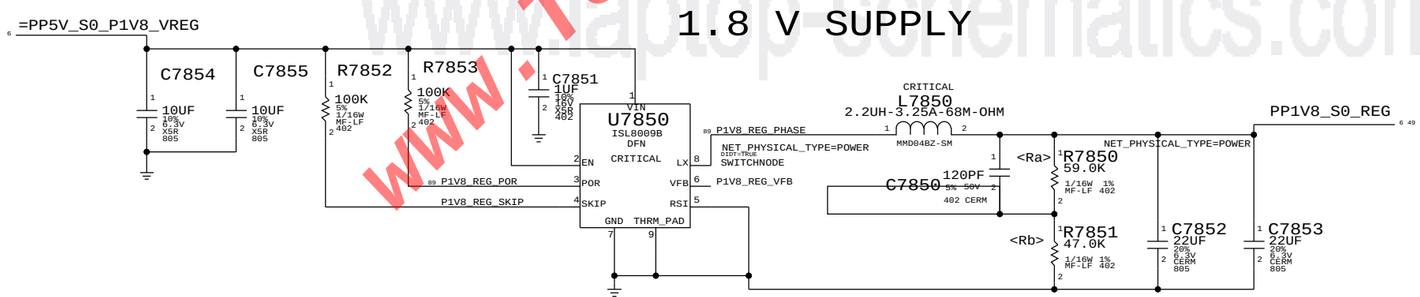


SYNC MASTER=K60_JERRY	SYNC DATE=07/01/2009
PAGE TITLE	5V_S3 / 3V3_S5 VREGS
Apple Inc.	DRAWING NUMBER 051-8233 SIZE D
	REVISION B.0.0
	BRANCH
	PAGE 77 OF 110
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

1.5 V DDR SUPPLY



1.8 V SUPPLY



SYNC MASTER=K60_JERRY SYNC DATE=07/01/2009

PAGE TITLE: 1.5V / 1.8V VREGS

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

REVISION: B.0.0

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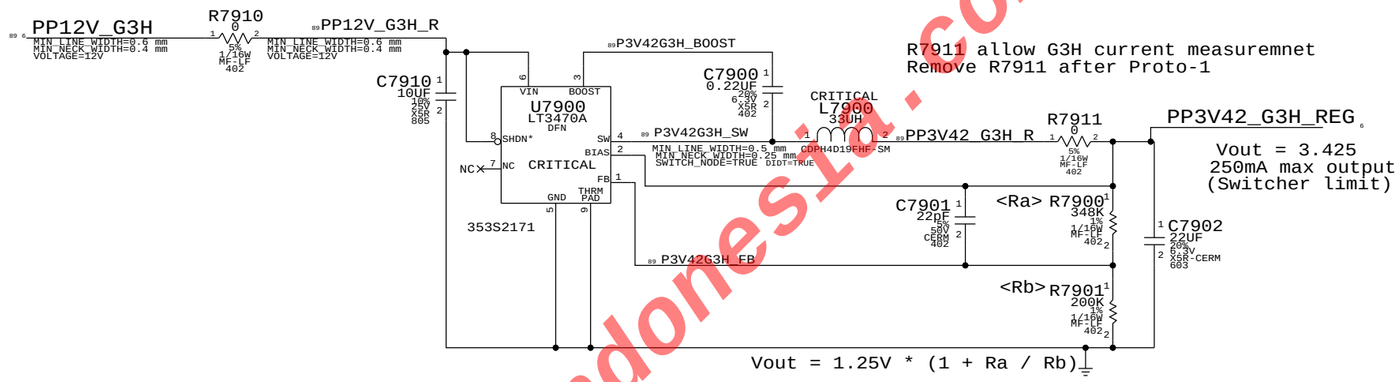
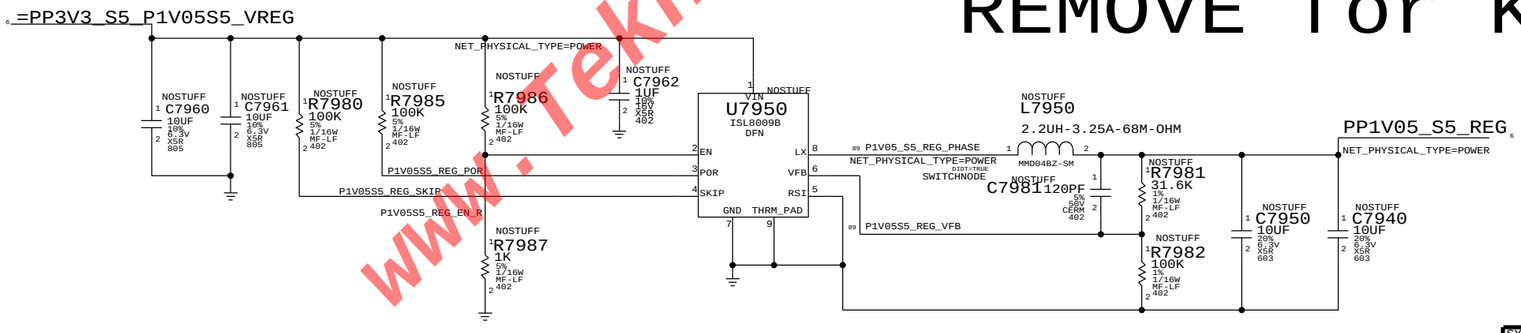
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



1.05V S5 SUPPLY



REMOVE for K60/K61

SYNC MASTER=K60 JERRY SYNC DATE=07/01/2009

PAGE TITLE: 1.05 S5 SUPPLY

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

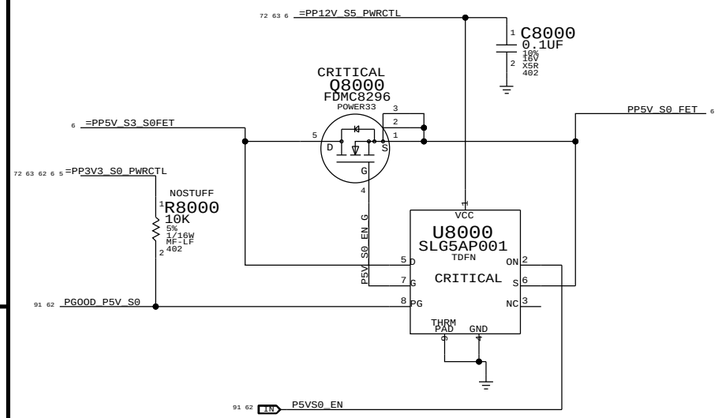
REVISION: B.0.0

BRANCH:

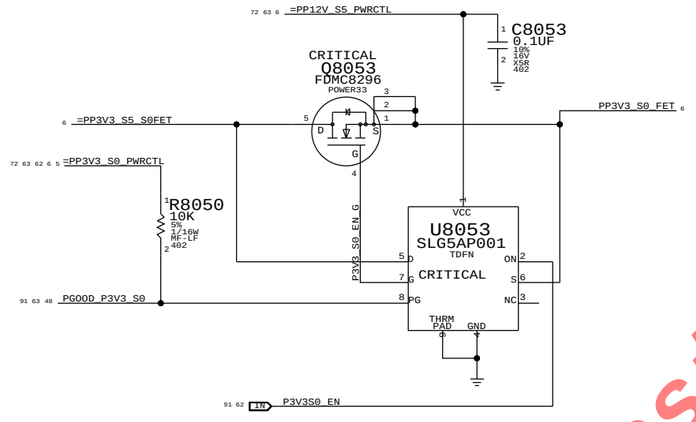
PAGE: 79 OF 110

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

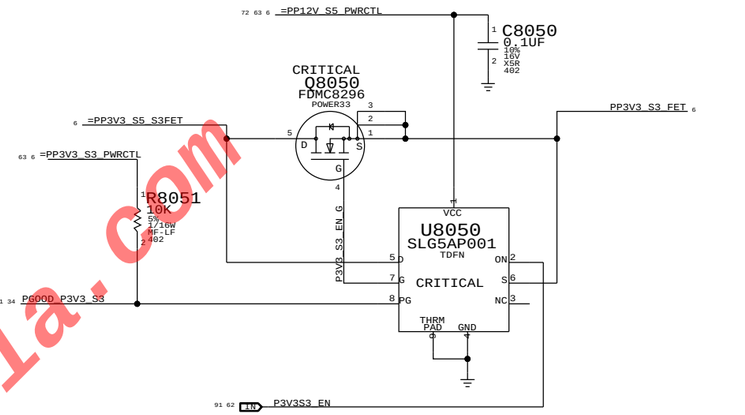
5V S0 FET (7A PK/2.7A AVG)



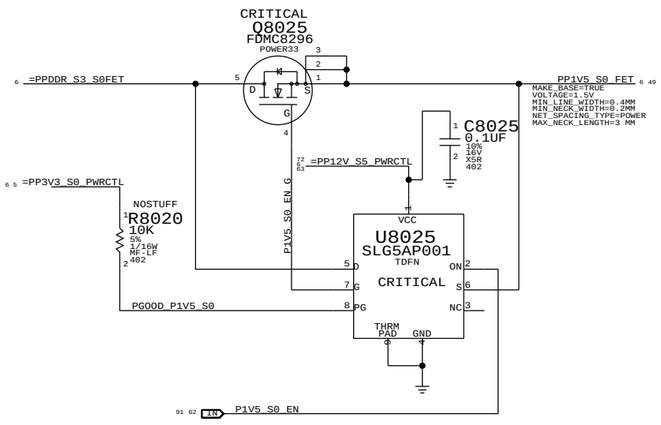
3.3V S0 FET (3.4APK / 1.9A AVG)



3.3V S3 FET (2.9A PK / 1.2A AVG)

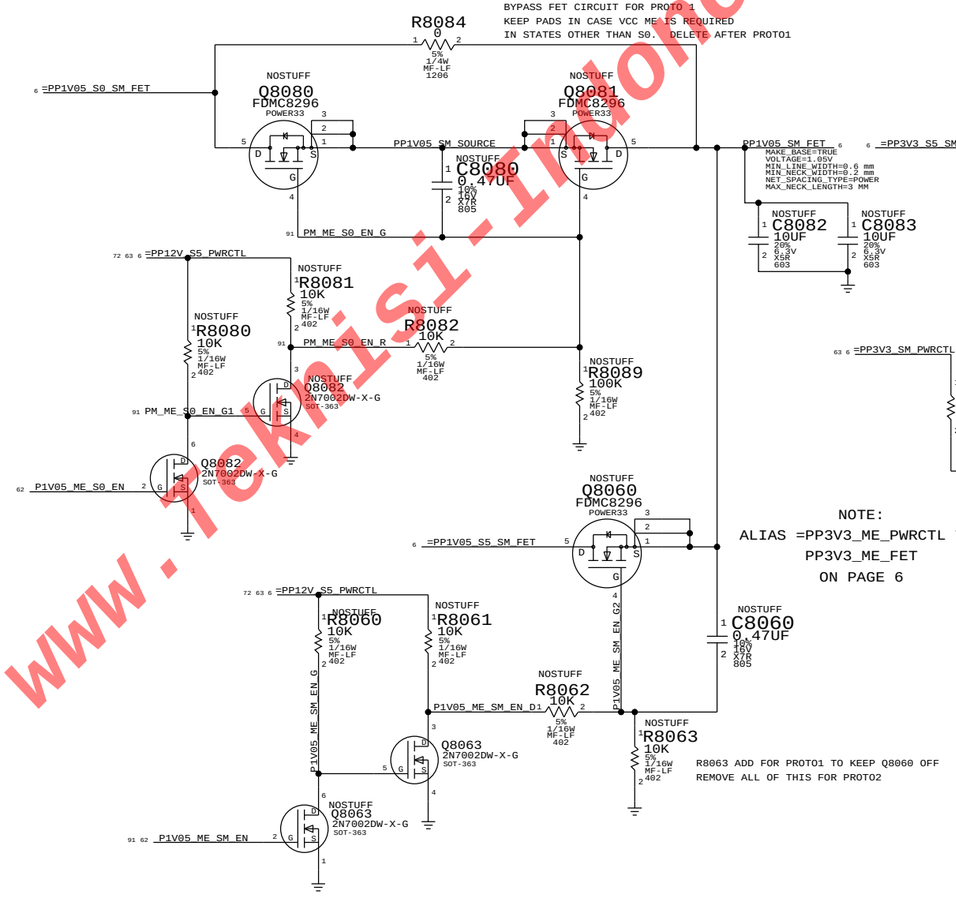


1.5V S0 FET (6.2A PK / 3A AVG)



1V05 ME FETS (S0: 2.2A MAX SM: 387MA)

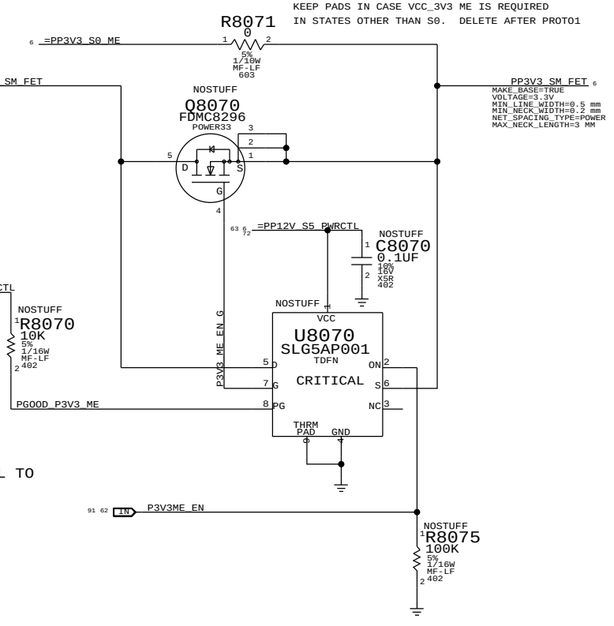
BYPASS FET CIRCUIT FOR PROTO 1
KEEP PADS IN CASE VCC_ME IS REQUIRED
IN STATES OTHER THAN S0. DELETE AFTER PROTO1



R8063 ADD FOR PROTO1 TO KEEP Q8060 OFF
REMOVE ALL OF THIS FOR PROTO2

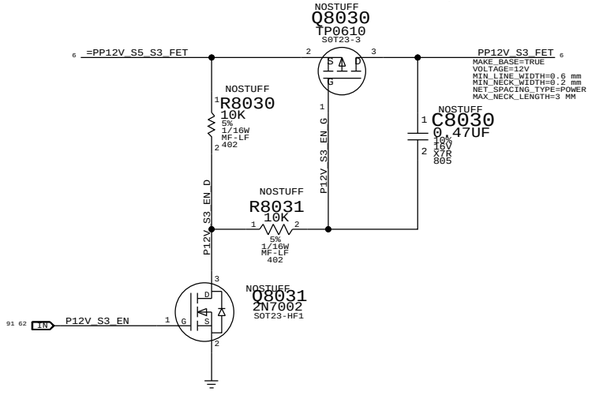
3.3VME FET (86MA MAX)

BYPASS FET CIRCUIT FOR PROTO 1
KEEP PADS IN CASE VCC_3V3 ME IS REQUIRED
IN STATES OTHER THAN S0. DELETE AFTER PROTO1



NOTE:
ALIAS =PP3V3_ME_PWRCTL TO
PP3V3_ME_FET
ON PAGE 6

12V S3 FET (< 200MA)



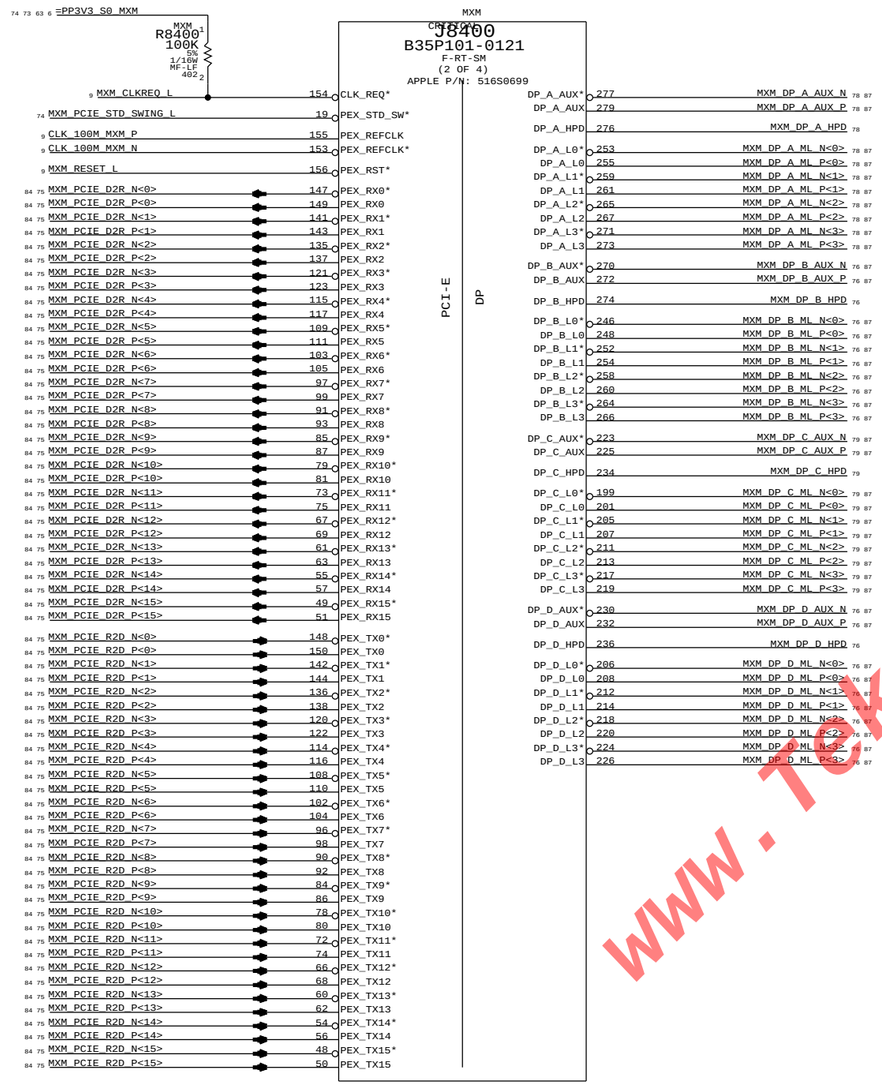
SYNC_MASTER=K60_MIKE	SYNC_DATE=07/01/2009
PAGE TITLE	S3+S0 FETS
Apple Inc.	DRAWING NUMBER 051-8233 · SIZE D · REVISION B.0.0 · BRANCH · PAGE 80 OF 110 · SHEET

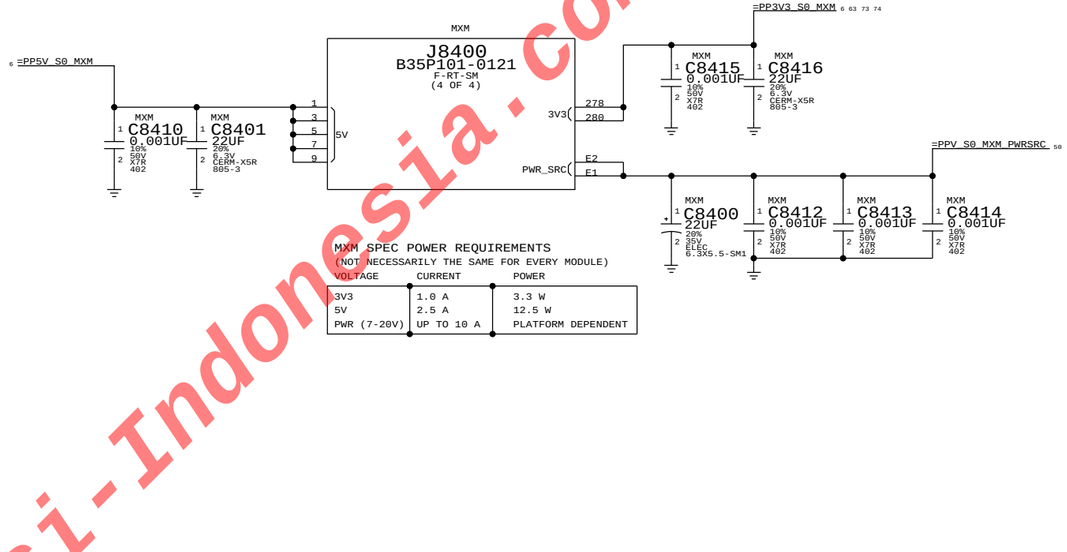
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM





MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

SYNC MASTER=K23_AARON SYNC DATE=07/16/2009

PAGE TITLE
MXM PCIe, DP & Power

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
REVISION B.0.0
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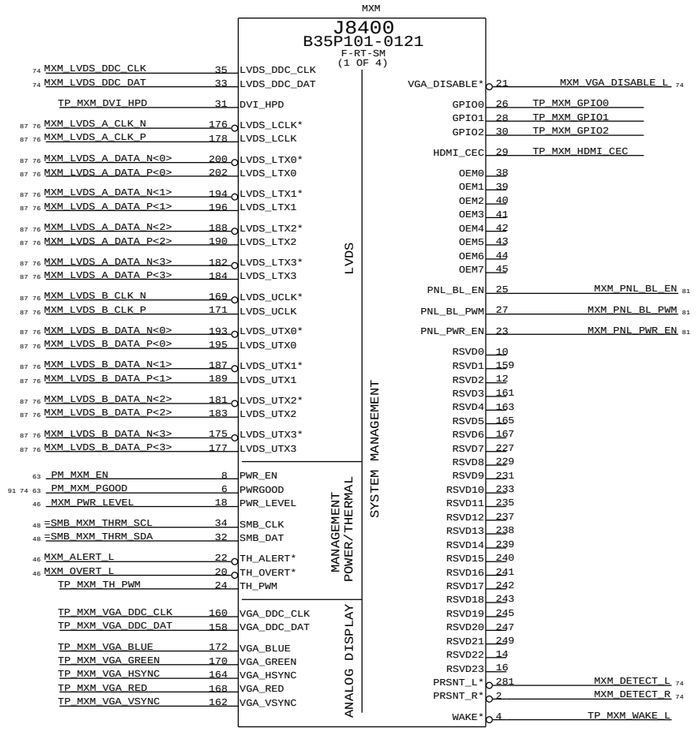
PAGE 84 OF 110
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

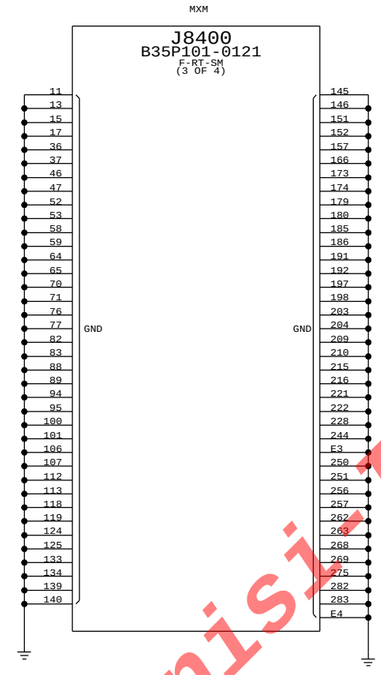
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM

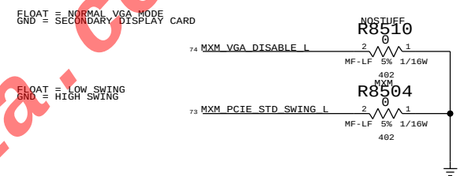
Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =SMB_MXM_THRM_CLK
- =PM_MXM_PGOOD_PULLUP

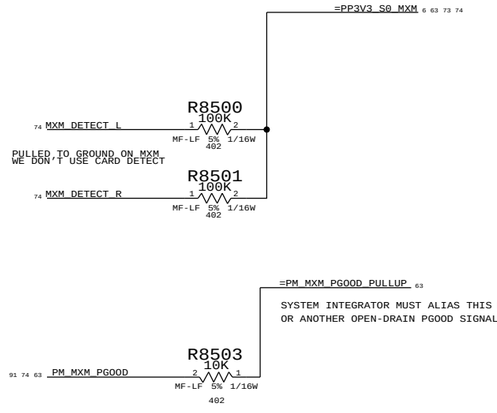
BOM options provided by this page:



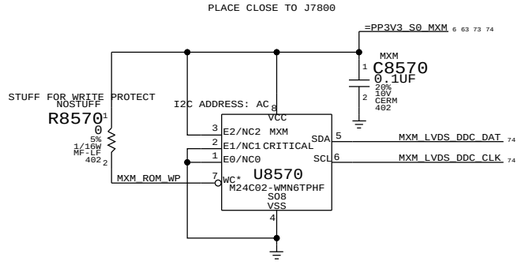


PULLUPS & PULLDOWNS AT MXM CONNECTOR





MXM SYSTEM INFORMATION ROM



SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE: MXM I/O

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D
REVISION: B.0.0
BRANCH:
PAGE: 85 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MXM TX CAPS

84 9	IN	PEG_R2D_C_P<0>	MXM	C8600	0.1UF	1 | 2	10% 16V X5R 402	MXM_PCIE_R2D_P<15>	OUT 73 84
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MXM RX CAPS

84 73	IN	MXM_PCIE_D2R_P<15>	MXM	C8632	0.1UF	1 | 2	10% 16V X5R 402	PEG_D2R_N<0>	OUT 9 84
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84 73	IN	MXM_PCIE_D2R_P<9>	MXM	C8644	0.1UF	1 | 2	10% 16V X5R 402	PEG_D2R_N<6>	OUT 9 84
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84 73	IN	MXM_PCIE_D2R_P<8>	MXM	C8646	0.1UF	1 | 2	10% 16V X5R 402	PEG_D2R_N<7>	OUT 9 84
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84 73	IN	MXM_PCIE_D2R_N<1>	MXM	C8663	0.1UF	1 | 2	10% 16V X5R 402	PEG_D2R_N<14>	OUT 9 84
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SYNC_MASTER=K60_AARON SYNC_DATE=07/01/2009

PAGE TITLE

MXM PCIE CAPS

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D

REVISION B.0.0

BRANCH

PAGE 86 OF 110

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- =PP3V3_S0_DP

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Unused MXM Interfaces

87 74	MXM_LVDS_A_CLK_N	NC_MXM_LVDS_A_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_CLK_P	NC_MXM_LVDS_A_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_N<0>	NC_MXM_LVDS_A_DATA_N<0>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_P<0>	NC_MXM_LVDS_A_DATA_P<0>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_N<1>	NC_MXM_LVDS_A_DATA_N<1>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_P<1>	NC_MXM_LVDS_A_DATA_P<1>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_N<2>	NC_MXM_LVDS_A_DATA_N<2>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_P<2>	NC_MXM_LVDS_A_DATA_P<2>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_N<3>	NC_MXM_LVDS_A_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_P<3>	NC_MXM_LVDS_A_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_CLK_N	NC_MXM_LVDS_B_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_CLK_P	NC_MXM_LVDS_B_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_N<0>	NC_MXM_LVDS_B_DATA_N<0>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_P<0>	NC_MXM_LVDS_B_DATA_P<0>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_N<1>	NC_MXM_LVDS_B_DATA_N<1>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_P<1>	NC_MXM_LVDS_B_DATA_P<1>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_N<2>	NC_MXM_LVDS_B_DATA_N<2>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_P<2>	NC_MXM_LVDS_B_DATA_P<2>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_N<3>	NC_MXM_LVDS_B_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_P<3>	NC_MXM_LVDS_B_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE

Unused MXM DP Interfaces

87 73	MXM_DP_B_ML_P<0..3>	NC_MXM_DP_B_ML_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_B_ML_N<0..3>	NC_MXM_DP_B_ML_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_B_AUX_P	NC_MXM_DP_B_AUX_P	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_B_AUX_N	NC_MXM_DP_B_AUX_N	MAKE_BASE=TRUE NO_TEST=TRUE
73	MXM_DP_B_HPD	NC_MXM_DP_B_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_D_ML_P<0..3>	NC_MXM_DP_D_ML_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_D_ML_N<0..3>	NC_MXM_DP_D_ML_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_D_AUX_P	NC_MXM_DP_D_AUX_P	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_D_AUX_N	NC_MXM_DP_D_AUX_N	MAKE_BASE=TRUE NO_TEST=TRUE
73	MXM_DP_D_HPD	NC_MXM_DP_D_HPD	MAKE_BASE=TRUE NO_TEST=TRUE

Display: Aliases

SYNC_MASTER=K61_AARON SYNC_DATE=07/01/2009

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7997	3.0.0
SCALE: NONE	SHT 76 OF 92	

Page Notes

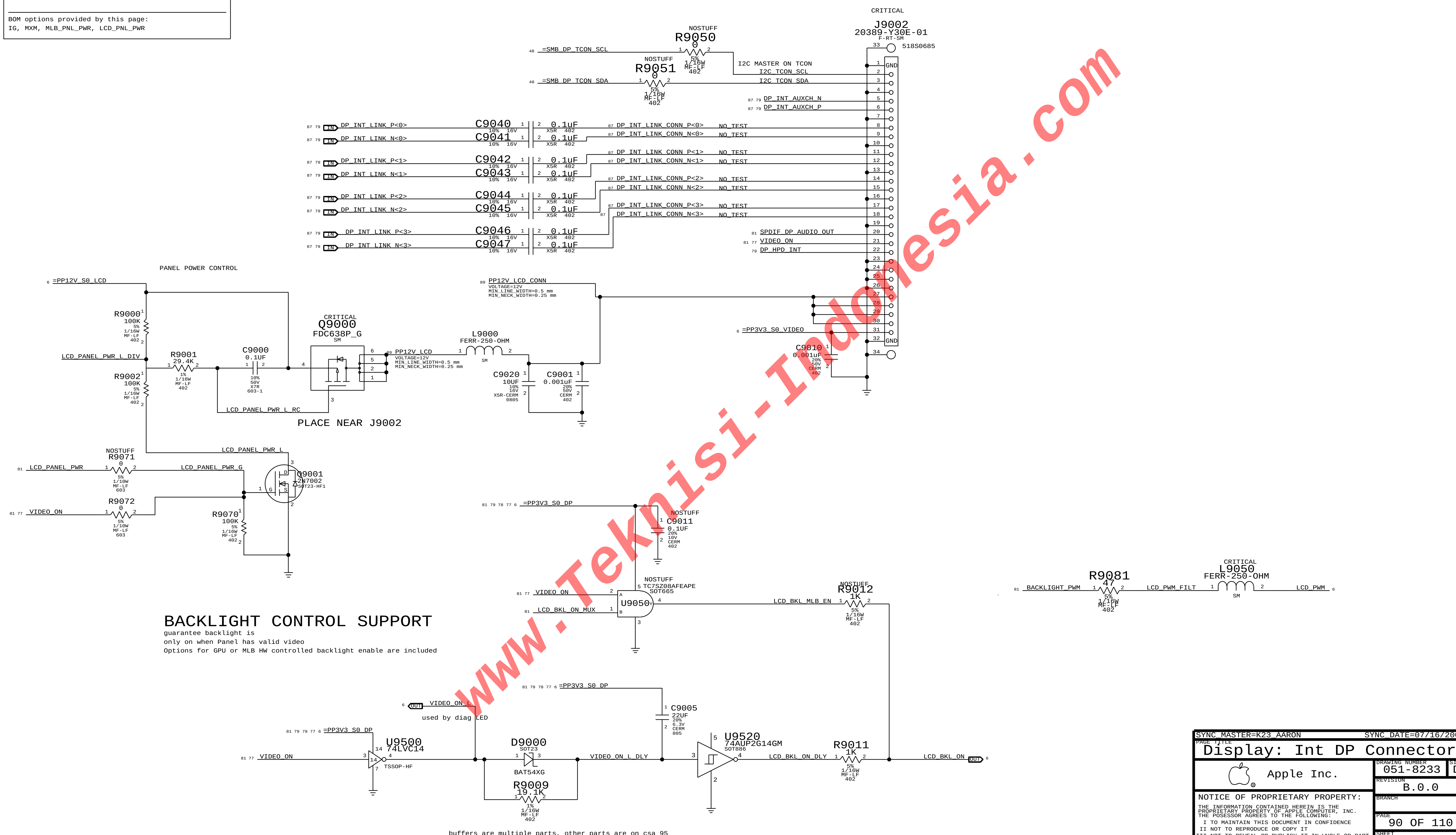
Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE



CRITICAL
J9002
20389-Y30E-01
F-RT-SM
518S0685
NOSTUFF
R9050
=SMB_DP_TCON_SCL
R9051
=SMB_DP_TCON_SDA
I2C MASTER ON TCON
I2C_TCON_SCL
I2C_TCON_SDA
DP_INT_AUXCH_N
DP_INT_AUXCH_P
DP_INT_LINK_P<0>
DP_INT_LINK_N<0>
DP_INT_LINK_P<1>
DP_INT_LINK_N<1>
DP_INT_LINK_P<2>
DP_INT_LINK_N<2>
DP_INT_LINK_P<3>
DP_INT_LINK_N<3>
C9040
C9041
C9042
C9043
C9044
C9045
C9046
C9047
0.1uF
DP_INT_LINK_CONN_P<0>
DP_INT_LINK_CONN_N<0>
DP_INT_LINK_CONN_P<1>
DP_INT_LINK_CONN_N<1>
DP_INT_LINK_CONN_P<2>
DP_INT_LINK_CONN_N<2>
DP_INT_LINK_CONN_P<3>
DP_INT_LINK_CONN_N<3>
NO_TEST
SPDIF_DP_AUDIO_OUT
VIDEO_ON
DP_HPD_INT
=PP3V3_S0_VIDEO
C9010
0.001uF
PANEL POWER CONTROL
=PP12V_S0_LCD
R9000
100K
LCD_PANEL_PWR_L_DIV
R9001
29.4K
C9000
0.1UF
R9002
100K
CRITICAL
Q9000
FDC638P_G
PP12V_LCD
L9000
FERR-250-OHM
PP12V_LCD_CONN
C9020
10UF
C9001
0.001uF
LCD_PANEL_PWR_L_RC
PLACE NEAR J9002
LCD_PANEL_PWR_L
NOSTUFF
R9071
LCD_PANEL_PWR
LCD_PANEL_PWR_G
Q9001
2N7002
SOT23-HF1
R9072
VIDEO_ON
R9070
100K
=PP3V3_S0_DP
C9011
0.1UF
TC7SZ08AFEAPE
SOT665
U9050
LCD_BKL_ON_MUX
LCD_BKL_MLB_EN
R9012
1K
R9081
47
BACKLIGHT_PWM
LCD_PWM_FILT
CRITICAL
L9050
FERR-250-OHM
LCD_PWM
BACKLIGHT CONTROL SUPPORT
guarantee backlight is
only on when Panel has valid video
Options for GPU or MLB HW controlled backlight enable are included
VIDEO_ON_L
used by diag LED
C9005
22UF
U9500
74LVC14
TSSOP-HF
D9000
SOT23
BAT54XG
VIDEO_ON_L_DLY
U9520
74AUP2G14GM
SOT886
LCD_BKL_ON_DLY
R9011
1K
LCD_BKL_ON
R9009
19.1K
buffers are multiple parts, other parts are on csa 95

SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE: Display: Int DP Connector

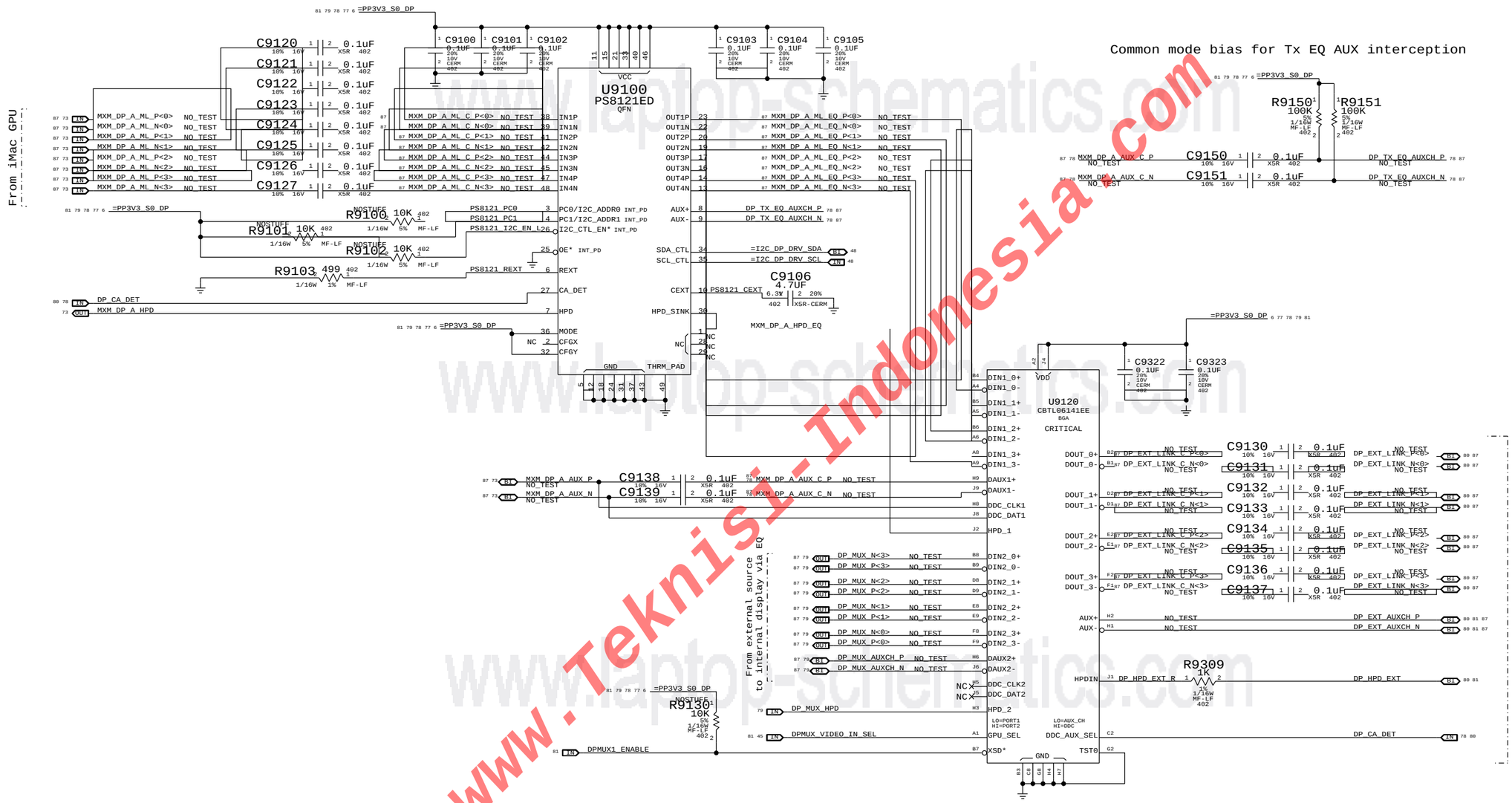
Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D

REVISION: B.0.0

BRANCH

EQ & Re-Driver for DP source



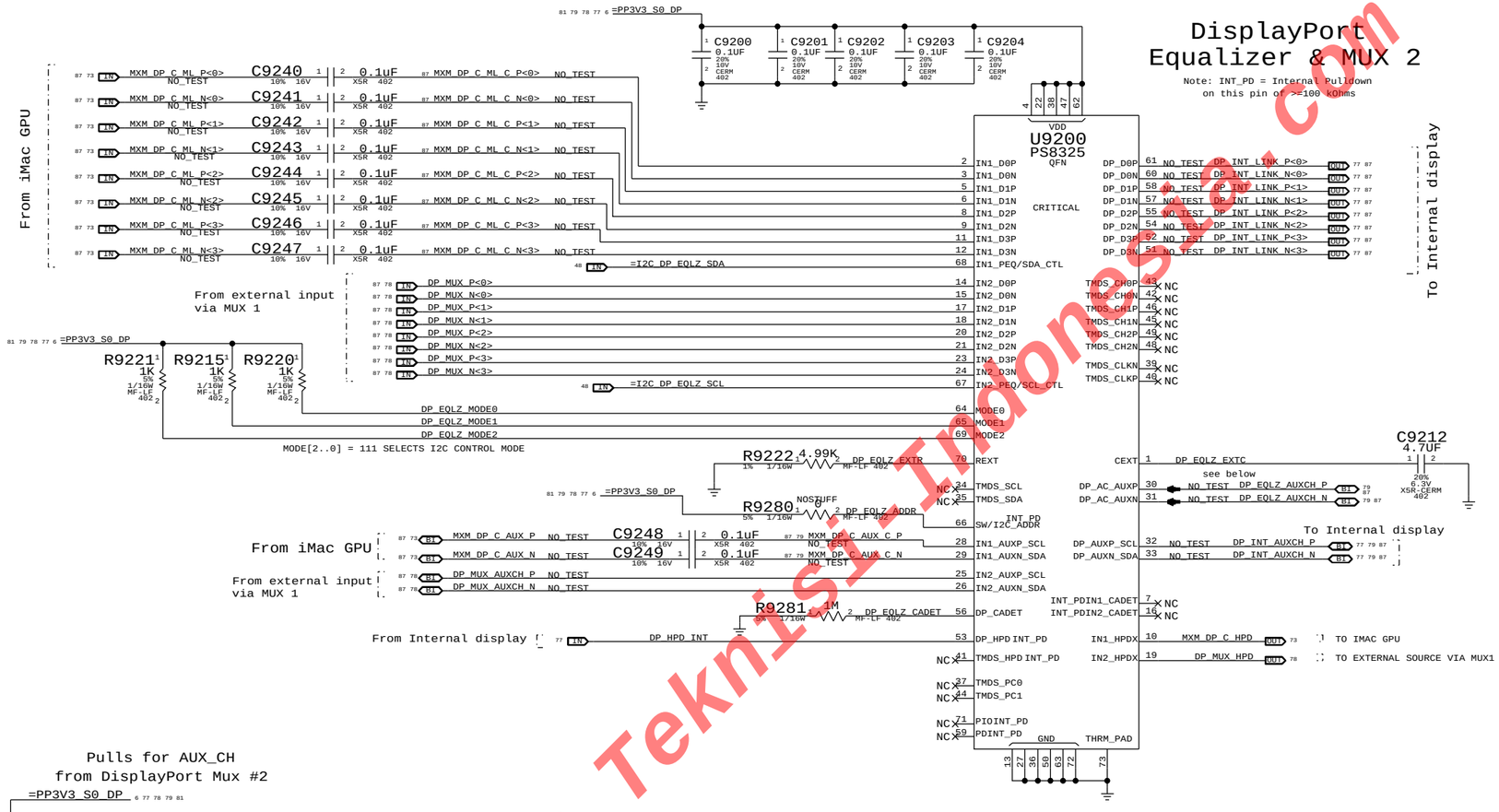
Common mode bias for Tx EQ AUX interception

DisplayPort Mux 1
Analog mux at External Connector

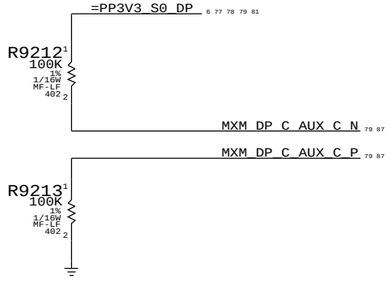
SYNC_MASTER=K23_AARON	SYNC_DATE=07/16/2009
PAGE TITLE: Display: BiDiVi Mux1	
Apple Inc.	DRAWING NUMBER: 051-8233 SIZE: D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	REVISION: B.0.0 BRANCH: PAGE: 91 OF 110 SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

DisplayPort Equalizer & MUX 2

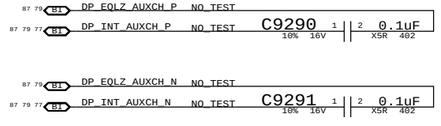
Note: INT_PD = Internal Pulldown on this pin of >=100 kOhms



Pulls for AUX_CH from DisplayPort Mux #2



AC caps for EQ AUX interception



SYNC_MASTER=K23_AARON	SYNC_DATE=07/16/2009
PAGE TITLE	BIDIVI DP MUX2
Apple Inc.	DRAWING NUMBER 051-8233 · SIZE D
	REVISION B.0.0
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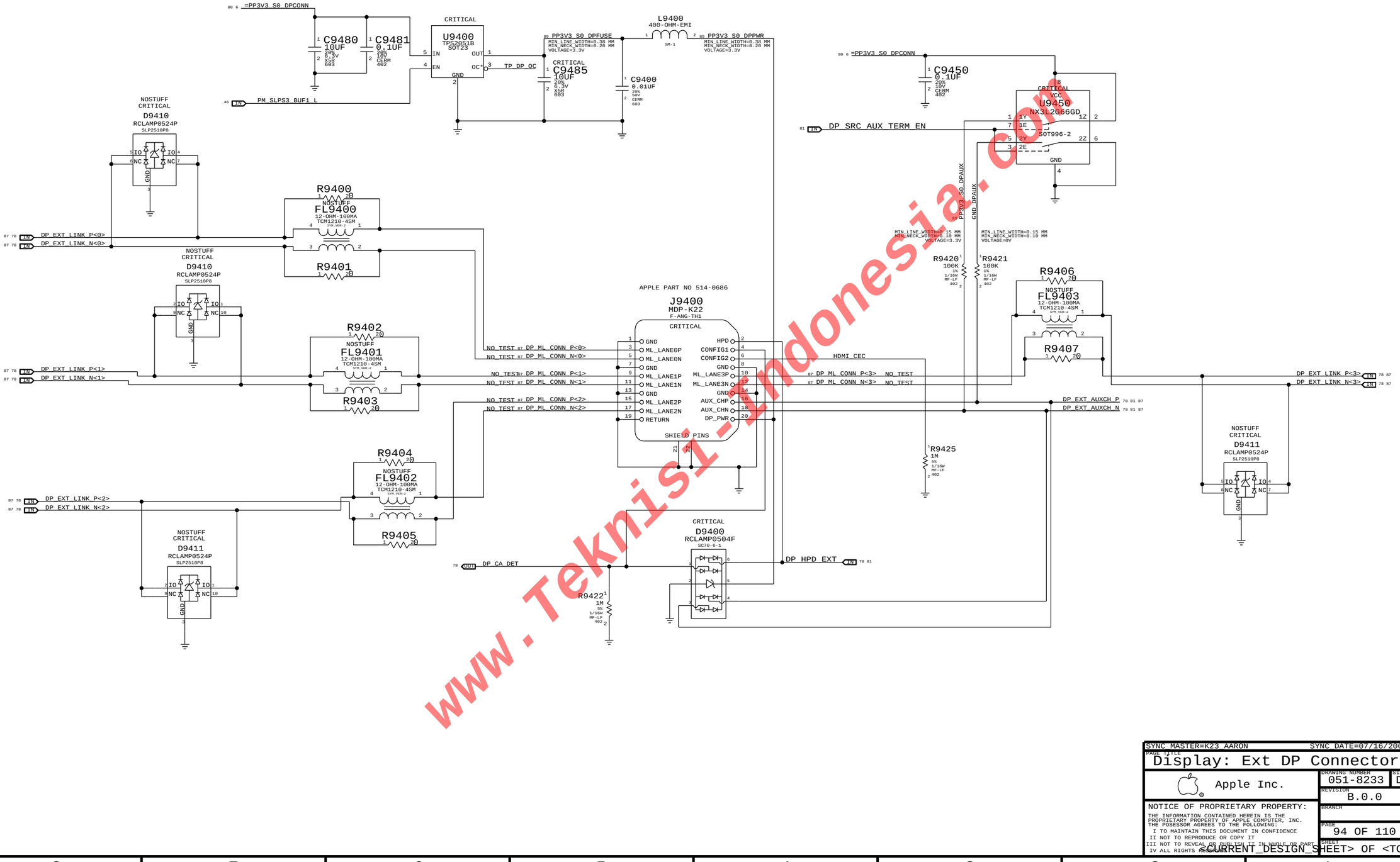
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE
DisPlay: Ext DP Connector

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
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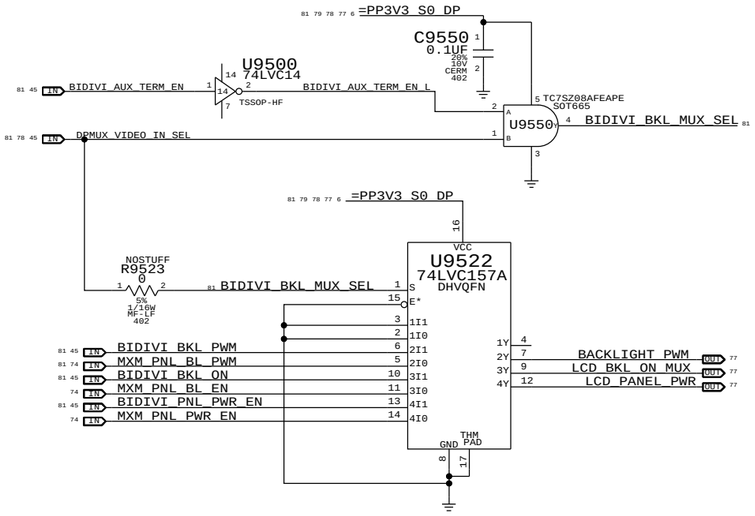
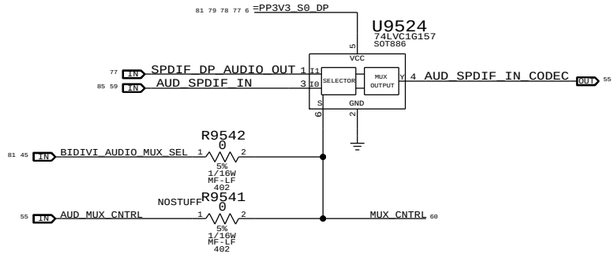
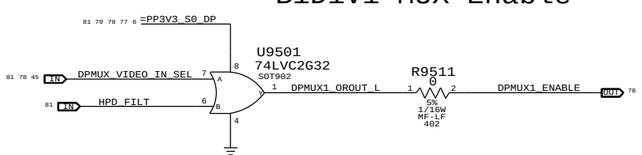
PANEL/BACKLIGHT CONTROL MUX



DisplayPort AUDIO MUX PLACE NEAR U6201

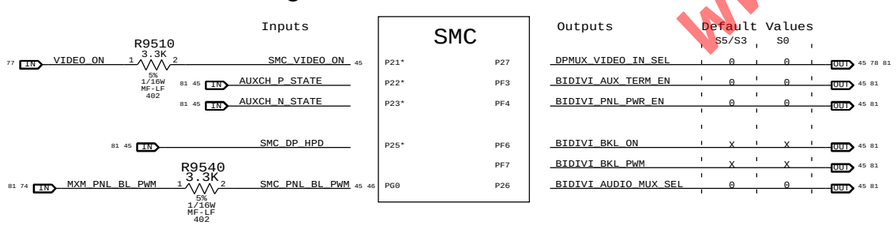


BiDiVi MUX Enable

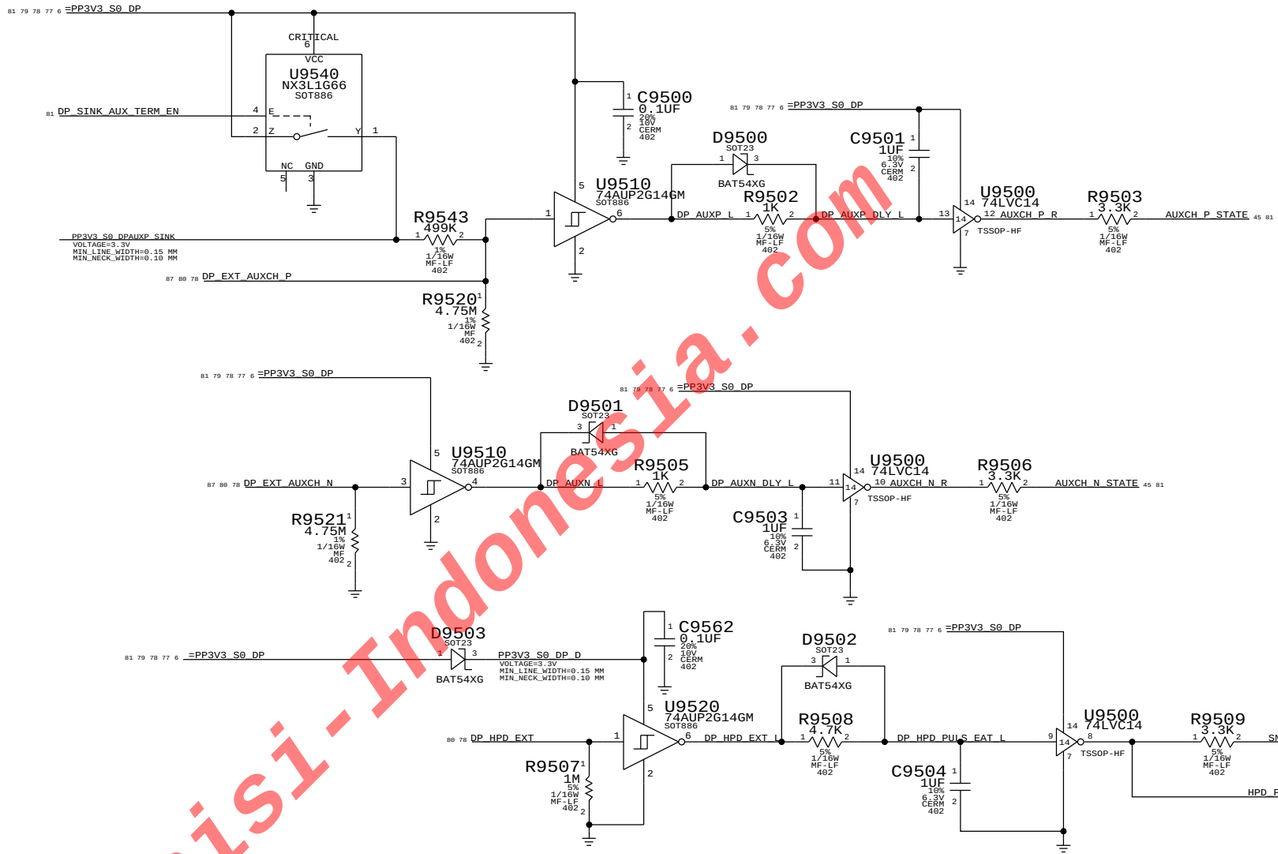


*Some inputs listed below come up as outputs driven low under the SMC flasher
Series R should prevent any issues on the inputs
Ouptuts are OK as low by default

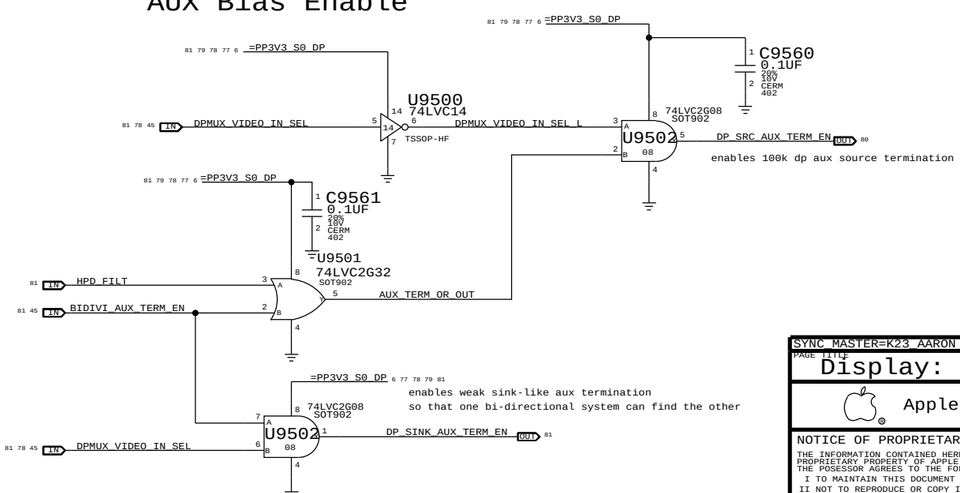
SMC Signals for BiDiVi



External AUX Channel and HPD Buffers & filters



AUX Bias Enable



*Some inputs listed below come up as outputs driven low under the SMC flasher
Series R should prevent any issues on the inputs
Ouptuts are OK as low by default

SYNC_MASTER=K23_AARON SYNC_DATE=07/16/2009

PAGE TITLE: Display: BiDiVi Support

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D
REVISION: B.0.0
BRANCH:
PAGE: 95 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

K60/K61 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OF MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.21 MM	0.085 MM	=STANDARD		
35_OHM_SE	*	Y	0.19 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD		
39_OHM_SE	*	Y	0.16 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD		
45_OHM_SE	*	Y	0.12 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL6	Y	0.115 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.085 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_CTL	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	BGA_P1MM	POWER_CTL
POWER	*	POWER_WIDTH
VR_CTL_PHY	BGA_P1MM	DEFAULT
VR_CTL_PHY	*	POWER_CTL

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?
6:1_SPACING	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.8 MM	1000

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.150 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.160 MM	?
3X_DIELECTRIC	*	0.220 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.240 MM	?
4X_DIELECTRIC	*	0.300 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.320 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.400 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	*	*	STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	STANDARD

K60/K61 RULE DEFINITIONS

SYNC_MASTER=K60_DEREK SYNC_DATE=07/01/2009

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7997	3.0.0

SCALE: NONE SHT 82 OF 92

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_4SS	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
MEM_35S	*	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DQ_ODD2DQ_ODD	*	=3:1_SPACING	?
MEM_DQ_ODD2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_EVEN	*	=3:1_SPACING	?
MEM_DQ_EVEN2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_ODD	*	=5:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DQ_ODD	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM
MEM_CLK	MEM_DQ_EVEN	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_ODD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_EVEN	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_ODD	MEM_CLK	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_CTRL	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_CMD	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_DQ_ODD	*	MEM_DQ_ODD2DQ_ODD
MEM_DQ_ODD	MEM_DQS	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_ODD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_EVEN	MEM_CLK	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_CTRL	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_CMD	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_EVEN
MEM_DQ_EVEN	MEM_DQS	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_DQ_ODD	*	MEM_DQ_EVEN2DQ_ODD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQ_ODD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQ_EVEN	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DQ_ODD	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM
MEM_CMD	MEM_DQ_EVEN	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DQ_ODD	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER
MEM_DQ_EVEN	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_POWER_WIDTH	*	Y	0.500 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_POWER_PHY	*	MEM_POWER_WIDTH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_POWER	*	0.2 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_RCOMP_PHY	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_RCOMP	*	0.2 MM	?

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	MEM_70D	MEM_CLK	MEM_A_CLK_P<3..0>	12 32
	MEM_70D	MEM_CLK	MEM_A_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_A_CKE<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_CS_L<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_ODT<3..0>	12 30
	MEM_35S	MEM_CMD	MEM_A_A<15..0>	12 30
	MEM_35S	MEM_CMD	MEM_A_BA<2..0>	12 30
	MEM_35S	MEM_CMD	MEM_A_RAS_L	12 30
	MEM_35S	MEM_CMD	MEM_A_CAS_L	12 30
	MEM_35S	MEM_CMD	MEM_A_WE_L	12 30
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<7..0>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<0>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<15..8>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<1>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<23..16>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<2>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<31..24>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<3>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<39..32>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<4>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<47..40>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<5>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<55..48>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<6>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<63..56>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<7>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	12 32
	MEM_70D	MEM_CLK	MEM_B_CLK_P<3..0>	12 32
	MEM_70D	MEM_CLK	MEM_B_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_B_CKE<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_CS_L<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_ODT<3..0>	12 31
	MEM_35S	MEM_CMD	MEM_B_A<15..0>	12 31
	MEM_35S	MEM_CMD	MEM_B_BA<2..0>	12 31
	MEM_35S	MEM_CMD	MEM_B_RAS_L	12 31
	MEM_35S	MEM_CMD	MEM_B_CAS_L	12 31
	MEM_35S	MEM_CMD	MEM_B_WE_L	12 31
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<7..0>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<0>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<15..8>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<1>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<23..16>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<2>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<31..24>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<3>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<39..32>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<4>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<47..40>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<5>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<55..48>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<6>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<63..56>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<7>	12 32

MEMORY POWER PROPERTIES

VOLTAGE	NET_TYPE PHYSICAL	SPACING		
1V5	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_A	12 28
1V5	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_B	12 28
1V8	MEM_POWER_PHY	MEM_POWER	VREFMARGIN_DIMMA_DQ	28
1V8	MEM_POWER_PHY	MEM_POWER	VREFMARGIN_DIMMB_DQ	28
1V8	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_A_SW	28
1V8	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_B_SW	28

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	12 32
1V8	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP0	11
1V8	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP1	11
1V8	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP2	11
1V8	MEM_70D	MEM_DQS	TP_MEM_B_DQS_P<8>	8 12
1V8	MEM_70D	MEM_DQS	TP_MEM_B_DQS_N<8>	8 12
1V8	MEM_70D	MEM_DQS	TP_MEM_A_DQS_P<8>	8 12
1V8	MEM_70D	MEM_DQS	TP_MEM_A_DQS_N<8>	8 12

ADD RULES TO NC_DQS<8>
TO CLEAR CHECK_PLUS ERRORS

SYNC_MASTER=K60_MIKE SYNC_DATE=07/01/2009

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: 051-8233 SIZE: D
REVISION: B.0.0
BRANCH:
PAGE: 101 OF 110
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=4X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_ITP	*	0.2 MM	?
CPU_RCOMP	*	0.2 MM	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=5X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5X_DIELECTRIC	?

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
FDI_MISC			
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>
	CPU_50S	CPU_AGTL	FDI_INT
SATA SSD			
	SATA_85D	SATA	SATA_SSD_R2D_C_P 18 42
	SATA_85D	SATA	SATA_SSD_R2D_C_N 18 42
	SATA_85D	SATA	SATA_SSD_R2D_P 42
	SATA_85D	SATA	SATA_SSD_R2D_N 42
	SATA_85D	SATA	SATA_SSD_D2R_P 18 42
	SATA_85D	SATA	SATA_SSD_D2R_N 18 42
	SATA_85D	SATA	SATA_SSD_D2R_C_P 42
	SATA_85D	SATA	SATA_SSD_D2R_C_N 42
CLOCKS			
	CLK_PCIE_100D	CLK_PCIE	DMI_MIDBUS_CLK100M_P 10 18
	CLK_PCIE_100D	CLK_PCIE	DMI_MIDBUS_CLK100M_N 10 18
CPU ITP			
	CPU_50S	CPU_ITP	XDP_BPM_L<7..0> 11 25
	CPU_50S	CPU_ITP	CPU_CFG<17..0> 10 15 25
	CPU_50S	CPU_ITP	XDP_OBSDATA_A<3..0> 25
CPU_MISC			
	CPU_50S	CPU_RCOMP	CPU_PEG_COMP 10
	CPU_50S	CPU_RCOMP	CPU_PEG_RBIAS 10
	CPU_50S	CPU_RCOMP	CPU_COMP3 11
	CPU_50S	CPU_RCOMP	CPU_COMP2 11
	CPU_50S	CPU_RCOMP	CPU_COMP1 11
	CPU_50S	CPU_RCOMP	CPU_COMP0 11

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
PCIE GRAPHICS			
	PCIE_85D	PCIE	PEG_R2D_C_P<15..0> 9 75
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0> 9 75
	PCIE_85D	PCIE	PEG_D2R_P<15..0> 9 75
	PCIE_85D	PCIE	PEG_D2R_N<15..0> 9 75
	PCIE_85D	PCIE	MXM_PCIE_R2D_P<15..0> 73 75
	PCIE_85D	PCIE	MXM_PCIE_R2D_N<15..0> 73 75
	PCIE_85D	PCIE	MXM_PCIE_D2R_P<15..0> 73 75
	PCIE_85D	PCIE	MXM_PCIE_D2R_N<15..0> 73 75
PCIE I/O			
	PCIE_85D	PCIE	PCIE_MINI_R2D_P 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_N 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_P 18 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_N 18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_P 18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_N 18 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_L_P 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_L_N 33
	PCIE_85D	PCIE	PCIE_FW_R2D_P 39
	PCIE_85D	PCIE	PCIE_FW_R2D_N 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_P 18 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N 18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_P 18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N 18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N 39
DMI			
	PCIE_85D	PCIE	DMI_S2N_P<3..0> 10 19
	PCIE_85D	PCIE	DMI_S2N_N<3..0> 10 19
	PCIE_85D	PCIE	DMI_N2S_P<3..0> 10 19
	PCIE_85D	PCIE	DMI_N2S_N<3..0> 10 19
FDI			
	PCIE_85D	PCIE	FDI_DATA_N<7..0>
	PCIE_85D	PCIE	FDI_DATA_P<15..0>
PCIE REF CLOCKS			
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P 9
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N 9
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_P 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_N 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P 18 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N 18 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P 18 39
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N 18 39
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_P 18 36
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_N 18 36
SATA			
	SATA_85D	SATA	SATA_HDD_R2D_C_P 18 42
	SATA_85D	SATA	SATA_HDD_R2D_C_N 18 42
	SATA_85D	SATA	SATA_HDD_R2D_P 42 92
	SATA_85D	SATA	SATA_HDD_R2D_N 42 92
	SATA_85D	SATA	SATA_HDD_D2R_P 18 42
	SATA_85D	SATA	SATA_HDD_D2R_N 18 42
	SATA_85D	SATA	SATA_HDD_D2R_C_P 42 92
	SATA_85D	SATA	SATA_HDD_D2R_C_N 42 92
	SATA_85D	SATA	SATA_ODD_R2D_C_P 18 42
	SATA_85D	SATA	SATA_ODD_R2D_C_N 18 42
	SATA_85D	SATA	SATA_ODD_R2D_P 42 92
	SATA_85D	SATA	SATA_ODD_R2D_N 42 92
	SATA_85D	SATA	SATA_ODD_D2R_P 18 42
	SATA_85D	SATA	SATA_ODD_D2R_N 18 42
	SATA_85D	SATA	SATA_ODD_D2R_C_P 42 92
	SATA_85D	SATA	SATA_ODD_D2R_C_N 42 92
CLOCKS			
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_CPU_P 11 21
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_CPU_N 11 21
	CLK_PCIE_100D	CLK_PCIE	GFX_CLK120M_DPLLSS_P 11 18
	CLK_PCIE_100D	CLK_PCIE	GFX_CLK120M_DPLLSS_N 11 18
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_ITP_P 11 25
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_ITP_N 11 25
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_CPU_P 11 18
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_CPU_N 11 18
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_PCH_P 18 26
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_PCH_N 18 26
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_PCH_P 18 26
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_PCH_N 18 26
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK96M_DOT_P 18 26
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK96M_DOT_N
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK100M_SATA_P 18 26
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK100M_SATA_N 18 26

SYNC_MASTER=K60_SIJI SYNC_DATE=07/01/2009

PAGE TITLE
PCIE/DMI/FDI/SATA CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8233 SIZE D
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SHEET

PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	0.2 MM	?
COMP_PCH	*	0.2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCI_5SS	PCI	PCI_REQ0_L	20
	PCI_5SS	PCI	PCI_REQ1_L	20
	CLK_PCI_5SS	CLK_PCI	PCH_CLK33M_PCIOUT	18 27
	CLK_PCI_5SS	CLK_PCI	PCH_CLK33M_PCIIN	18 27
	LPC_5SS	LPC	LPC_AD<3..0>	18 45 47
	LPC_5SS	LPC	LPC_FRAME_L	18 45 47
	CLK_LPC_5SS	CLK_LPC	LPC_CLK33M_SMC_R	20 27
	CLK_LPC_5SS	CLK_LPC	LPC_CLK33M_SMC	27 45
	CLK_LPC_5SS	CLK_LPC	LPC_CLK33M_LPCPLUS	27 47
	CLK_LPC_5SS	PM	PM_CLK32K_SUSCLK_R	9 19 91
	CLK_LPC_5SS	PM	PM_CLK32K_SUSCLK	9 45 91
	CLK_LPC_5SS	CLK_LPC	LPC_CLK33M_LPCPLUS_R	20 27
	USB_90D	USB	USB_EXTA_P	34 43
	USB_90D	USB	USB_EXTA_N	34 43
	USB_90D	USB	USB_PORT0_P	43
	USB_90D	USB	USB_PORT0_N	43
	USB_90D	USB	USB_EXTB_P	35 43
	USB_90D	USB	USB_EXTB_N	35 43
	USB_90D	USB	USB_PORT1_P	43
	USB_90D	USB	USB_PORT1_N	43
	USB_90D	USB	USB_EXTC_P	34 43
	USB_90D	USB	USB_EXTC_N	34 43
	USB_90D	USB	USB_PORT2_P	43
	USB_90D	USB	USB_PORT2_N	43
	USB_90D	USB	USB_EXTD_P	35 43
	USB_90D	USB	USB_EXTD_N	35 43
	USB_90D	USB	USB_D_MUXED_P	43
	USB_90D	USB	USB_D_MUXED_N	43
	USB_90D	USB	USB_PORT3_P	43
	USB_90D	USB	USB_PORT3_N	43
	USB_90D	USB	USB_CAMERA_P	34 44
	USB_90D	USB	USB_CAMERA_N	34 44
	USB_90D	USB	USB_CAMERA_L_P	44 92
	USB_90D	USB	USB_CAMERA_L_N	44 92
	USB_90D	USB	USB_BT_P	35 44
	USB_90D	USB	USB_BT_N	35 44
	USB_90D	USB	USB_BT_L_P	44 92
	USB_90D	USB	USB_BT_L_N	44 92
	USB_90D	USB	USB_IR_P	34 44
	USB_90D	USB	USB_IR_N	34 44
	USB_90D	USB	USB_IR_L_P	44 92
	USB_90D	USB	USB_IR_L_N	44 92
	USB_90D	USB	USB_SDCARD_P	35 44
	USB_90D	USB	USB_SDCARD_N	35 44
	USB_90D	USB	USB_SDCARD_L_P	44 92
	USB_90D	USB	USB_SDCARD_L_N	44 92
	USB_90D	USB	USB_WM_P	20 44
	USB_90D	USB	USB_WM_N	20 44
	USB_90D	USB	USB_WM_L_P	44
	USB_90D	USB	USB_WM_L_N	44
	USB_90D	USB	USB_MINI_P	
	USB_90D	USB	USB_MINI_N	
	USB_90D	USB	USB_BRCRYPT_P	20 44
	USB_90D	USB	USB_BRCRYPT_N	20 44
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	18 27
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	18 27
	CLK_XTAL	XTAL	CK505_XTAL_IN	26
	CLK_XTAL	XTAL	CK505_XTAL_OUT	26
	CLK_PCH_5SS	CLK_PCH	PCH_CLK14P3M_REFCLK	18 26
	USB_90D	USB	USB_BRCRYPT_L_P	44
	USB_90D	USB	USB_BRCRYPT_L_N	44
	USB_90D	USB	USB_HUB1_UP_P	20 34
	USB_90D	USB	USB_HUB1_UP_N	20 34
	USB_90D	USB	USB_HUB2_UP_P	20 35
	USB_90D	USB	USB_HUB2_UP_N	20 35

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SPI_5SS	SPI	SPI_CLK_R	18 47 54
	SPI_5SS	SPI	SPI_CLK	54
	SPI_5SS	SPI	SPI_MOSI_R	18 47 54
	SPI_5SS	SPI	SPI_MOSI	54
	SPI_5SS	SPI	SPI_MISO	18 47 54
	SPI_5SS	SPI	SPI_MISO_R	54
	SPI_5SS	SPI	SPI_CS0_R_L	18 47
	SPI_5SS	SPI	SPI_CS0_L	47
	SPI_5SS	SPI	SPI_MLB_CS_L	47 54
	SPI_5SS	SPI	SPI_ALT_CS_L	47
	SPI_5SS	SPI	SPIROM_USE_MLB	21 47
	SPI_5SS	SPI	SPI_ALT_MOSI	47
	SPI_5SS	SPI	SPI_ALT_MISO	47
	SPI_5SS	SPI	SPI_ALT_CLK	47
	HDA_5SS	HDA	HDA_BIT_CLK	18 55
	HDA_5SS	HDA	HDA_BIT_CLK_R	18
	HDA_5SS	HDA	HDA_RST_L	18 55
	HDA_5SS	HDA	HDA_RST_R_L	18
	HDA_5SS	HDA	HDA_SDOUT	18 55
	HDA_5SS	HDA	HDA_SDOUT_R	18
	HDA_5SS	HDA	HDA_SYNC	18 55
	HDA_5SS	HDA	HDA_SYNC_R	18
	HDA_5SS	HDA	HDA_SDIN0	18 55
	HDA_5SS	HDA	AUD_SDI_R	55
		HDA	AUD_SPDIF_IN	59 81
		HDA	AUD_SPDIF_OUT	55 59
		HDA	AUD_SPDIF_CHIP	55
	HDA_5SS	HDA	AUD_SPKR_OUTLO1L_NOUT	57 59 92
	HDA_5SS	HDA	AUD_SPKR_OUTLO1L_POUT	57 59 92
	HDA_5SS	HDA	AUD_SPKR_OUTLO1R_NOUT	57 59 92
	HDA_5SS	HDA	AUD_SPKR_OUTLO1R_POUT	57 59 92
	HDA_5SS	HDA	AUD_SPKR_OUTLO2L_NOUT	58 59 92
	HDA_5SS	HDA	AUD_SPKR_OUTLO2L_POUT	58 59 92
	HDA_5SS	HDA	AUD_SPKR_OUTLO2R_NOUT	58 59 92
	HDA_5SS	HDA	AUD_SPKR_OUTLO2R_POUT	58 59 92
	CLK_XTAL	XTAL	PCH_CLK25M_XTALOUT	18 27
	CLK_XTAL	XTAL	PCH_CLK25M_XTALIN	18 27
	PCH_5SS	COMP_PCH	PCH_USB_RBIAS	20
	PCH_5SS	COMP_PCH	PCH_SATAICOMP	18
	PCH_5SS	COMP_PCH	PCH_XCLK_RCOMP	18
	PCH_5SS	COMP_PCH	PCH_DMI_COMP	19
	CLK_XTAL	XTAL	USB_HUB1_XTAL1	34
	CLK_XTAL	XTAL	USB_HUB1_XTAL2	34
	PCH_5SS	COMP_PCH	USB_HUB1_RBIAS	34
	CLK_XTAL	XTAL	USB_HUB2_XTAL1	35
	CLK_XTAL	XTAL	USB_HUB2_XTAL2	35
	PCH_5SS	COMP_PCH	USB_HUB2_RBIAS	35

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IBEX PEAK CONSTRAINTS

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CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?
ENET_SE	*	=STANDARD	?

SOURCE:BROADCOM 5764M-DS04-RDS. PAGE 38

CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF	*	0.6 MM	?

SOURCE: BROADCOM 5764-DS04-RDS. PAGE 38

FireWire Interface Constraints

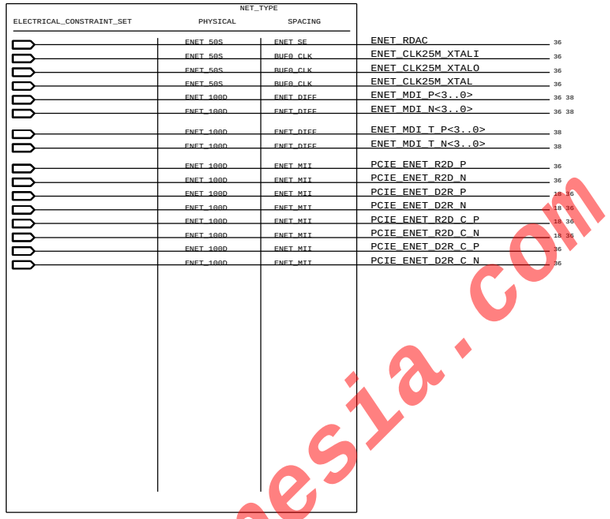
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

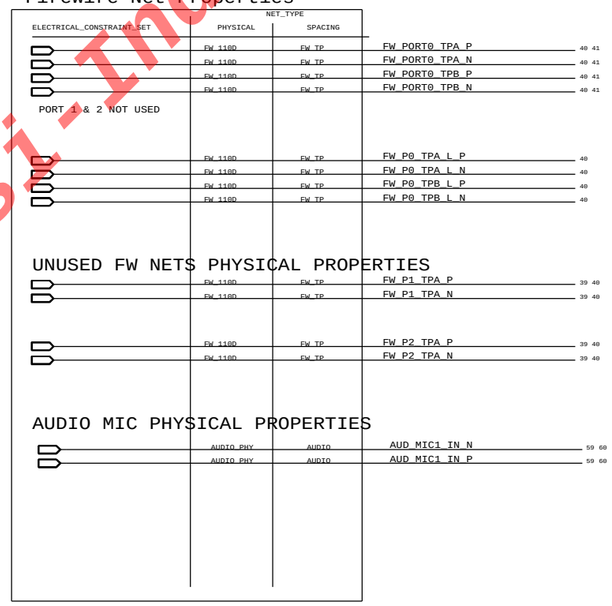
FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_PHY	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=STANDARD	?



FireWire Net Properties



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ENET/FIREWIRE CONSTRAINTS

Apple Inc.

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

PAIRS SHOULD BE WITHIN 100 MILS OF CLOCK LENGTH.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
ASSIGNED IN CONT. MGR.			
	DP_85D	DISPLAYPORT	DP_ML_CONN_P<3..0> 80
	DP_85D	DISPLAYPORT	DP_ML_CONN_N<3..0> 80
	DP_85D	DISPLAYPORT	DP_INT_LINK_CONN_P<3..0> 77
	DP_85D	DISPLAYPORT	DP_INT_LINK_CONN_N<3..0> 77
	DP_85D	DISPLAYPORT	DP_INT_LINK_P<3..0> 77 79
	DP_85D	DISPLAYPORT	DP_INT_LINK_N<3..0> 77 79
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_P 77 79
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_N 77 79
	DP_85D	DISPLAYPORT	DP_EXT_LINK_P<3..0> 78 80
	DP_85D	DISPLAYPORT	DP_EXT_LINK_N<3..0> 78 80
	DP_85D	DISPLAYPORT	DP_EXT_AUXCH_P 78 80 81
	DP_85D	DISPLAYPORT	DP_EXT_AUXCH_N 78 80 81
	DP_85D	DISPLAYPORT	DP_EXT_LINK_C_P<3..0> 78
	DP_85D	DISPLAYPORT	DP_EXT_LINK_C_N<3..0> 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_P<3..0> 73 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_N<3..0> 73 78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_C_P 78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_C_N 78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_P 73 78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_N 73 78
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_P<3..0> 73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_N<3..0> 73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_P 73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_N 73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_C_P 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_C_N 79
	DP_85D	DISPLAYPORT	DP_MUX_P<3..0> 78 79
	DP_85D	DISPLAYPORT	DP_MUX_N<3..0> 78 79
	DP_85D	DISPLAYPORT	DP_MUX_AUXCH_P 78 79
	DP_85D	DISPLAYPORT	DP_MUX_AUXCH_N 78 79
	DP_85D	DISPLAYPORT	DP_EQLZ_AUXCH_P 79
	DP_85D	DISPLAYPORT	DP_EQLZ_AUXCH_N 79
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_C_P<3..0> 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_C_N<3..0> 78
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_C_P<3..0> 79
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_C_N<3..0> 79
	DP_85D	DISPLAYPORT	DP_TX_EQ_AUXCH_P 78
	DP_85D	DISPLAYPORT	DP_TX_EQ_AUXCH_N 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_EQ_P<3..0> 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_EQ_N<3..0> 78

UNUSED VIDEO NET PHYSICAL CONSTRAINTS

	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_P 73 76
	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_N 73 76
	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_P 73 76
	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_N 73 76
	DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_P 74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_N 74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_P 74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_N 74 76
	DP_85D	DISPLAYPORT	MXM_DP_B_ML_P<3..0> 73 76
	DP_85D	DISPLAYPORT	MXM_DP_B_ML_N<3..0> 73 76
	DP_85D	DISPLAYPORT	MXM_DP_D_ML_P<3..0> 73 76
	DP_85D	DISPLAYPORT	MXM_DP_D_ML_N<3..0> 73 76
	DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_P<3..0> 74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_N<3..0> 74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_P<3..0> 74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_N<3..0> 74 76

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SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_5SS	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
THERMAL	POWER	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	48
	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	48
	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	48
	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	48
	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	48
	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	48
	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	48
	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	48
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	48 88
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	48 88
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	48 88
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	48 88
I136	SMB_5SS	SMB	SMBUS_PCH_S0_CLK	48
I135	SMB_5SS	SMB	SMBUS_PCH_S0_DATA	48
I160	SMB_5SS	SMB	SMBUS_PCH_CLK	18 48
I161	SMB_5SS	SMB	SMBUS_PCH_DATA	18 48
I137	SMB_5SS	SMB	SML_PCH_0_CLK	18 48
I139	SMB_5SS	SMB	SML_PCH_0_DATA	18 48
I138	SMB_5SS	SMB	SML_PCH_1_CLK	18 48
I140	SMB_5SS	SMB	SML_PCH_1_DATA	18 48
I127	CLK_XTAL	XTAL	SMC_EXTAL	45 46
I126	CLK_XTAL	XTAL	SMC_XTAL	45 46

SMC THERMAL NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I87	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	51 88
I88	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	51 88
I89	THERM_DIFF	THERMAL	SNS_T_DP2_DN3	51
I90	THERM_DIFF	THERMAL	SNS_T_DN2_DP3	51
I200	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	51 88
I201	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	51 88
I83	THERM_DIFF	THERMAL	SNS_T_DP4_DN5	51
I84	THERM_DIFF	THERMAL	SNS_T_DN4_DP5	51
I101	THERM_DIFF	THERMAL	SNS_LCD_P	51 92
I102	THERM_DIFF	THERMAL	SNS_LCD_N	51 92
I103	THERM_DIFF	THERMAL	SNS_ODD_P	51 92
I104	THERM_DIFF	THERMAL	SNS_ODD_N	51 92
I105	THERM_DIFF	THERMAL	SNS_CPU_H_P	51
I106	THERM_DIFF	THERMAL	SNS_CPU_H_N	51
I107	THERM_DIFF	THERMAL	SNS_SKIN_P	51 92
I108	THERM_DIFF	THERMAL	SNS_SKIN_N	51 92
I109	THERM_DIFF	THERMAL	SNS_AMB_P	51 92
I110	THERM_DIFF	THERMAL	SNS_AMB_N	51 92
I111	THERM_DIFF	THERMAL	SNS_MXM_P	51
I112	THERM_DIFF	THERMAL	SNS_MXM_N	51
I192	THERM_DIFF	THERMAL	SNS_CPU_THERMD_P	10 51
I193	THERM_DIFF	THERMAL	SNS_CPU_THERMD_N	10 51
I113		THERMAL	HDD_OOB_TEMP_FILT	51 92
I134		THERMAL	HDD_OOB_TEMP	51
I133		THERMAL	HDD_OOB_TEMP_R	51
I132		THERMAL	SMC_HDD_OOB_TEMP	51

SMC VOLTAGE/CURRENT NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I97	THERM_DIFF	THERMAL	MXM_ISENSE_P	50
I98	THERM_DIFF	THERMAL	MXM_ISENSE_N	50
I99	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S3_P	49
I100	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S3_N	49
I144	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S0_P	49
I145	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S0_N	49
I150	THERM_DIFF	THERMAL	SENSE_CPU_1V5_P	49
I151	THERM_DIFF	THERMAL	SENSE_CPU_1V5_N	49
I152	THERM_DIFF	THERMAL	SENSE_CPU_VTT_P	49
I153	THERM_DIFF	THERMAL	SENSE_CPU_VTT_N	49
I181	THERM_DIFF	THERMAL	SENSE_CPU_VTT1_P	
I182	THERM_DIFF	THERMAL	SENSE_CPU_VTT1_N	
I183	THERM_DIFF	THERMAL	SENSE_CPU_VTT2_P	
I184	THERM_DIFF	THERMAL	SENSE_CPU_VTT2_N	
I162		THERMAL	GND_SMC_AVSS	45 46 49 50
I124		THERMAL	SMC_CPU_1V5_ISENSE	46 49
I190		THERMAL	SMC_CPU_1V5_ISENSE_R	49
I122		THERMAL	SMC_CPU_1V5_VSENSE	46 49
I163		THERMAL	SMC_CPU_VTT_ISENSE	46 49
I164		THERMAL	SMC_CPU_VTT_ISENSE_R	49
I165		THERMAL	SMC_CPU_VTT_VSENSE	46 49
I166		THERMAL	SMC_CPU_1V8_ISENSE	46 49
I167		THERMAL	SMC_CPU_1V8_ISENSE_R	
I168		THERMAL	SMC_CPU_1V8_VSENSE	46 49
I120		THERMAL	SMC_CPU_VSENSE	45 49
I131	VID_PHY	VR_CTL	VR_CPU_IOUT	13 64
I130	THERM_DIFF	THERMAL	VR_ISNS_CPU_P	49
I129	THERM_DIFF	THERMAL	VR_ISNS_CPU_N	49
I128		THERMAL	SNS_PS_CPU_ISNS	49
I125		THERMAL	SMC_CPU_ISENSE	45 49
I169		THERMAL	SMC_CPU_INPUT_ISENSE	46
I172		THERMAL	SMC_CPU_INPUT_VSENSE	46
I173		THERMAL	SMC_DIMM_1V5_ISENSE	46 50
I174		THERMAL	SMC_1V5_S3_ISENSE_R	
I175		THERMAL	SMC_DIMM_1V5_VSENSE	46 50
I178		THERMAL	SMC_GPU_ISENSE	45 50
I179		THERMAL	SMC_MXM_ISENSE_R	50
I180		THERMAL	SMC_GPU_VSENSE	45 50

SYNC_MASTER=K60_JERRY SYNC_DATE=07/01/2009

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Apple Inc.

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SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SWITCHNODE	SWITCHNODE	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	BGA_P1MM	BGA_P2MM
SWITCHNODE	GND	BGA_P1MM	BGA_P2MM
SWITCHNODE	*	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	*	6:1_SPACING
SWITCHNODE	GND	*	6:1_SPACING
SWITCHNODE	*	*	SWITCHNODE

POWER NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING	VOLTAGE		
1720	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE1	65
1721	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE2	65
1722	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE3	65
1723	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE4	66
1724	POWER	SWITCHNODE	3.3V	P3V3S5_REG_PHASE	69
1725	POWER	SWITCHNODE	5V	P5VS3_REG_PHASE	69
1726	POWER	SWITCHNODE	1.1V	VTT_REG_PHASE1	67
1727	POWER	SWITCHNODE	1.1V	VTT_REG_PHASE2	67
1728	POWER	SWITCHNODE	3.4V	P3V42G3H_SW	71
1729	POWER	SWITCHNODE	1.05V	PCHCORE_REG_PHASE	68
1730	POWER	SWITCHNODE	1.05V	P1V05_S5_REG_PHASE	71
1431	POWER	SWITCHNODE	1.5V	DDR_REG_PHASE	70
1440	POWER	SWITCHNODE	1.8V	P1V8_REG_PHASE	70
1141	POWER	POWER	1.5V	PP0V75_S3_MEM_VREFCA_A	28 30
1142	POWER	POWER	1.5V	PP0V75_S3_MEM_VREFCA_B	28 31
1143	POWER	POWER	1.5V	PP0V75_S3_MEM_VREFDQ_A	28 30
1144	POWER	POWER	1.5V	PP0V75_S3_MEM_VREFDQ_B	28 31
1608	POWER	POWER	12V	PP12V_S0_CPUVTT_FLTD	
1649	POWER	POWER	12V	PP12V_AUD_SPKRAMP_PLANE	57 58 60
1640	POWER	POWER	12V	PP12V_LCD	77
1641	POWER	POWER	12V	PP12V_LCD_CONN	77
1645	POWER	POWER	12V	PP12V_S0	6 63
1646	POWER	POWER	12V	PP12V_S0_CPU_FLTRD	64 65 66
1647	POWER	POWER	12V	PP12V_S0_FAN0_L	52 92
1372	POWER	POWER	12V	PP12V_S0_FAN1_L	52 92
1373	POWER	POWER	12V	PP12V_S0_FAN2_L	53 92
1606	POWER	POWER	12V	PP12V_G3H	6 71
1609	POWER	POWER	12V	PP12V_G3H_R	71
1374	POWER	POWER	12V	PP12V_S5	6
1375	POWER	POWER	12V	P12V_S0_FW	64 65 66
1376	POWER	POWER	12V	P12V_S0_FW_CL	
1377	POWER	POWER	12V	P12V_S0_FW_D	
1378	POWER	POWER	12V	P12V_S0_FW_R	
1266	POWER	POWER	12V	FW_PORT0_VP	41
1267	POWER	POWER	12V	FW_PORT0_VP_F	41
1644	POWER	POWER	12V	PPVP_FW_PHY_CPS	40 41
1643	POWER	POWER	12V	PP12V_S3_WM_FLT	44
1655					6
1255	POWER	POWER	1.1V	PPVCORE_S0_CPU	6
1256	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG1	65
1257	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG2	65
1664	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG3	65
1665	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG4	66
1635	POWER	POWER	1.05V	PP1V05_SM_SOURCE	72
1637	POWER	POWER	1.05V	PP1V05_S0	6
1179	POWER	POWER	1.05V	PP1V05_S0_CK505_F	26
1180	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA	17 22
1181	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA_F	
1182	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB	17 22
1183	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB_F	
1184	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_EXP	22 24
1185	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_FDI	22 24
1186	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_SATA	22 24
1187	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCA_CLK	22 24
1188	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCA_CLK_F	24
1699	POWER	POWER	1.05V	PP1V05_S0_CIO_VDD1P0_DP	
1698	POWER	POWER	1.05V	PP1V05_S0_CIO_VDD1P0_DP_PLL	
1634	POWER	POWER	1.05V	PP1V05_SM_PCH_LAN	6
1632	POWER	POWER	1.05V	PP1V05_S5	6
1674	POWER	POWER	1.05V	PP1V05_SM	6
1260	POWER	POWER	1.1V	PPVTT_S0	6
1650	POWER	POWER	1.1V	PPVTT_S0_CPU	6 49
1261	POWER	POWER	0.75V	PPVTT_S0_DDR	6
1633	POWER	POWER	0.75V	PP0V75_S0	6
1190	POWER	POWER	1.2V	PP1V2_S5_ENET	37
1192	POWER	POWER	1.5V	PP1V5_S0	6
1193	POWER	POWER	1.5V	PP1V5_S0_CK505_F	26
1587	POWER	POWER	1.5V	PP1V5_S0_CK505_R	26
1195	POWER	POWER	1.5V	PP1V5_S3	6
1196	POWER	POWER	1.5V	PP1V5_CPU_MEM	6 49
1262	POWER	POWER	1.5V	PP1V8R1V5_S0_PCH_VCCVRM	22 24
1197	POWER	POWER	1.5V	PP1V5_FW_VDDA	39
1263	POWER	POWER	1.5V	PP1V8_S0	6
1264	POWER	POWER	1.8V	PP1V8_S0_CPU	6 49
1265	POWER	POWER	1.96V	PP1V96_FW_PLLVDD	39
1266	POWER	POWER	1.96V	PP1V95_FW_FWPHY	39 40

POWER NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING	VOLTAGE		
1210	POWER	POWER	3.3V	PP3V3_S0	6
1211	POWER	POWER	3.3V	PP3V3_S0_CK505_F	26
1213	POWER	POWER	3.3V	PP3V3_S0_DPAUX	80
1215	POWER	POWER	3.3V	PP3V3_S0_DPFUSE	80
1222	POWER	POWER	3.3V	PP3V3_S0_DPPWR	80
1221	POWER	POWER	3.3V	PP3V3_S0_HS_F	61
1670	POWER	POWER	3.3V	PP3V3_S0M	6
1681	POWER	POWER	3.3V	PP3V3_MINI	33
1612	POWER	POWER	3.3V	PP3V3_ENET	36 37
1223	POWER	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC	17 22
1224	POWER	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC_F	
1220	POWER	POWER	3.3V	PP3V3_S0_TSENS_R	51
1225	POWER	POWER	3.3V	PP3V3_S3	6 92
1557	POWER	POWER	3.3V	PP3V3_S3_BT_FLT	44
1238	POWER	POWER	3.3V	PP3V3_S3_SDCARD_FLT	44
1555	POWER	POWER	3.3V	PP3V3_S3_WM_FLT	44
1235	POWER	POWER	3.3V	PP3V3_S5	6
1227	POWER	POWER	3.3V	PPVTT_S3_DDR_BUF	70
1227	POWER	POWER	3.3V	PPV_S0_MXM_PWRSRC	50
1265	POWER	POWER	3.3V	PPVOUT_S0_PCH_DCPSST	22
1266	POWER	POWER	3.3V	PPVOUT_S5_PCH_DCPSUS	22
1267	POWER	POWER	3.3V	PPVOUT_S5_PCH_DCPSUSBYP	22
1629	POWER	POWER	3.3V	PPVOUT_G3_PCH_DCPRTC	22
1631				PPVOUT_SO_PCH_VCCRTC_NCTF	
1229	POWER	POWER	3.3V	PPVBATT_G3_RTC	27
1230	POWER	POWER	3.3V	PPVBATT_G3_RTC_R	27
1209	POWER	POWER	3.3V	PP3V3_AUDIO_SPDIF_JACK	59
1208	POWER	POWER	3.3V	PP3V3_FW_AVDD	39
1232	POWER	POWER	3.3V	PP3V3_FW_ESD	41
1231	POWER	POWER	3.3V	PP3V3_FW_PLLVDD	39
1233	POWER	POWER	3.3V	PP3V3_FW_VDDA	39
1211	POWER	POWER	3.3V	PP3V3_G3_RTC	18 22 24 27
1212	POWER	POWER	3.3V	PP_ENET_CTRL12	37
1239	POWER	POWER	3.4V	PP3V3_G3H_SMC_AVCC	45
1231	POWER	POWER	3.3V	PP3V3_G3H_AVREF_SMC	45 46
1606	POWER	POWER	3.42V	PP3V42_G3H	6
1607	POWER	POWER	3.42V	PP3V42_G3H_R	71
1577	POWER	POWER	4.5V	4V5_REG_IN	55
1236	POWER	POWER	4.5V	PP4V5_AUDIO_ANALOG	55
1237	POWER	POWER	5V	PP5V_S0	6 92
1238	POWER	POWER	5V	PP5V_S0_CPU_VCORE_VCC	64
1239	POWER	POWER	5V	PP5V_S0_PCH_VSREF	22 24
1603	POWER	POWER	5V	PP5V_S0_SATA_FET	45
1240	POWER	POWER	5V	PP5V_S3	6
1241	POWER	POWER	5V	PP5V_S3_DDR_REG_V5FILT	70
1636	POWER	POWER	5V	PP5V_S3_CAMERA_FLT	44
1243	POWER	POWER	5V	PP5V_S3_IR_FLT	44
1601	POWER	POWER	5V	VREFMARGIN_DIMMA_P5V	28
1600	POWER	POWER	5V	VREFMARGIN_DIMMB_P5V	28
1244	POWER	POWER	5V	PP5V_S5	6
1724	POWER	POWER	5V	PP5V_S5_PCH_VSREFSUS	22 24
1245	POWER	POWER	5V	PP5V_CPUVTT_VR	67
1247	POWER	POWER	5V	PP5V_USB2_PORT0	43
1246	POWER	POWER	5V	PP5V_USB2_PORT0_F	43
1248	POWER	POWER	5V	PP5V_USB2_PORT1	43
1249	POWER	POWER	5V	PP5V_USB2_PORT1_F	43
1250	POWER	POWER	5V	PP5V_USB2_PORT2	43
1252	POWER	POWER	5V	PP5V_USB2_PORT2_F	43
1253	POWER	POWER	5V	PP5V_USB2_PORT3	43
1255	POWER	POWER	5V	PP5V_USB2_PORT3_F	43
1645	POWER	POWER		DDR_REG_PGND	70
1646	POWER	POWER		DDR_REG_CSGND	70

SENSING NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING		
1150	SNS_DIFF	THERMAL	VR_CPU_ISNS1_P	64 65
1151	SNS_DIFF	THERMAL	VR_CPU_ISNS1_N	64 65
1152	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_P	64
1153	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_N	64
1154	SNS_DIFF	THERMAL	VR_CPU_ISNS2_P	64 65
1155	SNS_DIFF	THERMAL	VR_CPU_ISNS2_N	64 65
1161	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_P	64
1162	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_N	64
1163	SNS_DIFF	THERMAL	VR_CPU_ISNS3_P	64 65
1164	SNS_DIFF	THERMAL	VR_CPU_ISNS3_N	64 65
1165	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_P	64
1166	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_N	64
1167	SNS_DIFF	THERMAL	VR_CPU_ISNS4_P	64 66
1168	SNS_DIFF	THERMAL	VR_CPU_ISNS4_N	64 66
1169	SNS_DIFF	THERMAL	VR_CPU_ISNS4_R_P	64
1170	SNS_DIFF	THERMAL	VR_CPU_ISNS4_R_N	64
1660	SNS_DIFF	THERMAL	VR_CPU_ISNS1_XW_P	65
1661	SNS_DIFF	THERMAL	VR_CPU_ISNS1_XW_N	65
1662	SNS_DIFF	THERMAL	VR_CPU_ISNS2_XW_P	65
1663	SNS_DIFF	THERMAL	VR_CPU_ISNS2_XW_N	65
1670	SNS_DIFF	THERMAL	VR_CPU_ISNS3_XW_P	65
1671	SNS_DIFF	THERMAL	VR_CPU_ISNS3_XW_N	65
1672	SNS_DIFF	THERMAL	VR_CPU_ISNS4_XW_P	66
1673	SNS_DIFF	THERMAL	VR_CPU_ISNS4_XW_N	66
1676	SNS_DIFF		CPU_VCC_PKG_SENSE_P	13 49 64
1677	SNS_DIFF		CPU_VCC_PKG_SENSE_N	13 64
1156	SNS_DIFF		CPU_VTTSENSE_P	13 49 67
1157	SNS_DIFF		CPU_VTTSENSE_N	13 67
1172	SNS_DIFF		CPU_VTTSENSE_R_P	67
1173	SNS_DIFF		CPU_VTTSENSE_R_N	67
1158	SNS_DIFF		VR_CPU_VSEN	64
1159	SNS_DIFF		VR_CPU_RGND	64
1174	SNS_DIFF		VR_CPU_VSNS_R_N	64
1175	SNS_DIFF		VR_CPU_VSNS_R_P	64
1160	SNS_DIFF		VR_CPU_VSNS_XW_P	64
1161	SNS_DIFF		VR_CPU_VSNS_XW_N	64

VR CTRL NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING		
1727	VR_CTL_PHY	VR_CTL	VR_CPU_PH1_SNUB	65
1835	VR_CTL_PHY	VR_CTL	VR_CPU_PH2_SNUB	65
1839	VR_CTL_PHY	VR_CTL	VR_CPU_PH3_SNUB	65
1840	VR_CTL_PHY	VR_CTL	VR_CPU_PH4_SNUB	66
1841	VR_CTL_PHY	VR_CTL	VR_CPU_PWM1	64 65
1842	VR_CTL_PHY	VR_CTL	VR_CPU_PWM2	64 65
1843	VR_CTL_PHY	VR_CTL	VR_CPU_PWM2_R	64
1844	VR_CTL_PHY	VR_CTL	VR_CPU_PWM3	64 65
1845	VR_CTL_PHY	VR_CTL	VR_CPU_PWM3_R	64
1846	VR_CTL_PHY	VR_CTL	VR_CPU_PWM4	64 66
1847	VR_CTL_PHY	VR_CTL	VR_CPU_PWM4_R	64
1848	VR_CTL_PHY	VR_CTL	VR_CPU_REF	64
1849	VR_CTL_PHY	VR_CTL	VR_CPU_SS	64
1850	VR_CTL_PHY	VR_CTL	VR_CPU_TCOMP	64
1851	VR_CTL_PHY	VR_CTL	VR_CPU_TM	64
1852	VR_CTL_PHY	VR_CTL	VR_CPU_BOOT1_RC	65
1853	VR_CTL_PHY	VR_CTL	VR_CPU_BOOT2_RC	65
1854	VR_CTL_PHY	VR_CTL	VR_CPU_BOOT3_RC	65
1855	VR_CTL_PHY	VR_CTL	VR_CPU_COMP	64
1856	VR_CTL_PHY	VR_CTL	VR_CPU_COMP_R	64
1857	VR_CTL_PHY	VR_CTL	VR_CPU_COMP_RC	64
1858	VR_CTL_PHY	VR_CTL	VR_CPU_DAC	64
1859	VR_CTL_PHY	VR_CTL	VR_CPU_DRV1_BOOT	65
1860	VR_CTL_PHY	VR_CTL	VR_CPU_DRV1_GDSEL	65
1861	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV1_LGATE	65
1862	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV1_UGATE	65
1863	VR_CTL_PHY	VR_CTL	VR_CPU_DRV2_BOOT	65
1864	VR_CTL_PHY	VR_CTL	VR_CPU_DRV2_GDSEL	65
1865	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV2_LGATE	65
1866	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV2_UGATE	65
1867	VR_CTL_PHY	VR_CTL	VR_CPU_DRV3_BOOT	65
1868	VR_CTL_PHY	VR_CTL	VR_CPU_DRV3_GDSEL	65
1869	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV3_LGATE	65
1870	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV3_UGATE	65
1871	VR_CTL_PHY	VR_CTL	VR_CPU_DRV4_BOOT	66
1872	VR_CTL_PHY	VR_CTL	VR_CPU_DRV4_GDSEL	66
1873	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV4_LGATE	66
1874	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV4_UGATE	66
1875	VR_CTL_PHY	VR_CTL	VR_CPU_FAN	64
1876	VR_CTL_PHY	VR_CTL	VR_CPU_FB	64
1877	VR_CTL_PHY	VR_CTL	VR_CPU_FB_R	64
1878	VR_CTL_PHY	VR_CTL	VR_CPU_FS	64
1879	VR_CTL_PHY	VR_CTL	VR_CPU_IMON	49 64
1880	VR_CTL_PHY	VR_CTL	VR_CPU_IOUT_PD	64
1881	VR_CTL_PHY	SWITCHNODE	PCHCORE_REG_UGATE	68
1882	VR_CTL_PHY	SWITCHNODE	PCHCORE_REG_LGATE	68
1883	VR_CTL_PHY	VR_CTL	PCHCORE_REG_VFB	68
1884	VR_CTL_PHY	VR_CTL	PCHCORE_REG_TON	68
1885	VR_CTL_PHY	VR_CTL	PCHCORE_REG_TRIP	68
1886	VR_CTL_PHY	VR_CTL	PCHCORE_REG_BOOT	68
1887	VR_CTL_PHY	VR_CTL	PCHCORE_REG_BOOT_R	68
1888	VR_CTL_PHY	VR_CTL	VTT_REG_BOOT1	67
1889	VR_CTL_PHY	VR_CTL	VTT_REG_BOOT2	67
1890	VR_CTL_PHY	VR_CTL	VTT_REG_COMP	67
1891	VR_CTL_PHY	VR_CTL	VTT_REG_FB	67
1892	VR_CTL_PHY	VR_CTL	VTT_REG_FS	67
1893	VR_CTL_PHY	VR_CTL	VTT_REG_FCOMP	67
1894	VR_CTL_PHY	VR_CTL	VTT_REG_IREF	67
1895	VR_CTL_PHY	VR_CTL	VTT_REG_TSUM	67
1896	VR_CTL_PHY	SWITCHNODE	VTT_REG_LGATE1	67
1897	VR_CTL_PHY	SWITCHNODE	VTT_REG_LGATE2	67
1898	VR_CTL_PHY	VR_CTL	VTT_REG_OCSET	67
1899	VR_CTL_PHY	VR_CTL	VTT_OFST	67
1900	VR_CTL_PHY	VR_CTL	VTT_REG_REF	67
1901	VR_CTL_PHY	VR_CTL	VTT_REG_RGND	67
1902	VR_CTL_PHY	VR_CTL	VTT_SEL	67
1903	VR_CTL_PHY	VR_CTL	VTT_REG_UGATE2	67
1904	VR_CTL_PHY	VR_CTL	VTT_REG_UGATE1	67
1905	VR_CTL_PHY	VR_CTL	VTT_REG_PH1_SNUB	67
1906	VR_CTL_PHY	VR_CTL	VTT_REG_PH2_SNUB	67
1907	VR_CTL_PHY	VR_CTL	VTT_REG_VSEN	67
1159	VR_CTL_PHY	VR_CTL	P1V05S5_REG_VFB	71
1668	VR_CTL_PHY	VR_CTL	P3V42G3H_BOOST	71
1669	VR_CTL_PHY	VR_CTL	P3V42G3H_FB	71

VR CTRL NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING		
1634	VR_CTL_PHY	VR_CTL	DDR_REG_CS	70
1635	VR_CTL_PHY	VR_CTL	DDR_REG_FB	70
1636	VR_CTL_PHY	SWITCHNODE	DDR_REG_LGATE	70
1638	VR_CTL_PHY	SWITCHNODE	DDR_REG_UGATE	70
1639	VR_CTL_PHY	VR_CTL	DDR_REG_BOOT	70
1640	VR_CTL_PHY	VR_CTL	DDR_REG_BOOT_R	70
1641	VR_CTL_PHY	VR_CTL	DDR_REG_VDDQSNS	70
1642	VR_CTL_PHY	VR_CTL	DDR_REG_VTTSNS	70
1440	VR_CTL_PHY	VR_CTL	P1V8_REG_POR	70
1636	VR_CTL_PHY	VR_CTL	P3V3S5_REG_BOOT	69
1637	VR_CTL_PHY	VR_CTL	P3V3S5_REG_BOOT_R	69
1638	VR_CTL_PHY	VR_CTL	P3V3S5_REG_FB	69
1639	VR_CTL_PHY	VR_CTL	P3V3S5_REG_ISEN	69
1640	VR_CTL_PHY	SWITCHNODE	P3V3S5_REG_LGATE	69
1641	VR_CTL_PHY	VR_CTL	P3V3S5_REG_OCSET	69
1642	VR_CTL_PHY	SWITCHNODE	P3V3S5_REG_UGATE	69
1643	VR_CTL_PHY	VR_CTL	P3V3S5_REG_SNUB	69
1644	VR_CTL_PHY	VR_CTL	P5VS3_REG_BOOT	69
1645	VR_CTL_PHY	VR_CTL	P5VS3_REG_FB	69
1646	VR_CTL_PHY	VR_CTL	P5VS3_REG_ISEN	69
1647	VR_CTL_PHY	SWITCHNODE	P5VS3_REG_LGATE	69
1648	VR_CTL_PHY	VR_CTL	P5VS3_REG_OCSET	69
1649	VR_CTL_PHY	SWITCHNODE	P5VS3_REG_UGATE	69

VR VID NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING		
1650	VID_PHY	VR_CTL	CPU_VID<0>	13 16 64
1651	VID_PHY	VR_CTL	CPU_VID<1>	13 16 64
1652	VID_PHY	VR_CTL	CPU_VID<2>	13 16 64
1653	VID_PHY	VR_CTL	CPU_VID<3>	13 16 64
1654	VID_PHY	VR_CTL	CPU_VID<4>	13 16 64
1655	VID_PHY	VR_CTL	CPU_VID<5>	13 16 64
1656	VID_PHY	VR_CTL	CPU_VID<6>	13 16 64
1657	VID_PHY	VR_CTL	CPU_VID<7>	13 16 64
1658	VID_PHY	VR_CTL	CPU_PSI_L	13 16 64

PULL-UP STUB < 1-INCH
VID LENGTH SKEW < 1-INCH
VID LENGTH RANGE< 1 TO 15-INCH

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VID_PHY	*	39_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL	*	0.2MM	?

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POWER CONSTRAINTS

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PM NET PROPERTIES
(PM, RESET, EN, PGOOD)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2:1_SPACING
PM_VTT	PM_VTT	*	2:1_SPACING
PM_VTT	*	*	3:1_SPACING
PM_VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT

	NET_TYPE		
	PHYSICAL	SPACING	
P6	PM	PLT_RESET_L	20 27
P5	PM_VTT	PLT_RESET_LS1V1_L	11
P4	PM	PM_ACDC_PS_ON	6
P3	PM	PM_BATLOW_L	15 19 45
P8	PM	PM_CLK32K_SUSCLK	9 45 85
P9	PM	PM_CLK32K_SUSCLK_R	9 19 85
P7	PM	PM_CLKRUN_L	15 19 45 47
P6			
P148	PM	PM_EXT_TS_L<0>	11 46
P8	PM	PM_EXT_TS_L<1>	11 46
P147	PM	PM_LAN_PWRGD	15 19
P117	PM_VTT	FSB_CPURSTOUT_L	11 25
P120	PM	USB_HUB_RESET_L	34 35
P25	PM_VTT	PM_MEM_PWRGD	11 19
P24	PM	PM_ME_PWRGD	19 63
P27	PM	PM_ME_S0_EN_G	72
P26	PM	PM_ME_S0_EN_G1	72
P28	PM	PM_ME_S0_EN_R	72
P30	PM	PM_MXM_PGOOD	63 74
P29	PM	PM_PCH_PWRGD	19 63
P31	PM	PM_PGOOD_DDRREG_S3	5 62 70
P33	PM	PM_PGOOD_PVCORE_CPU	5 26 63 64
P32	PM	PM_PWRBTN_L	19 25 45
P35	PM	PM_RSMRST_L	45 62
P34	PM	PM_RSMRST_PCH_L	19 62
P36	PM	PM_SLP_M_L	5 19 62
P38	PM	PM_SLP_M_R	
P37	PM	PM_SLP_S3_L	5 19 32 33 37 46 62 63
P40	PM	PM_SLP_S3_L_AND_S0_RDY	
P120	PM	PM_SLP_S4_1_L	19 62
P119	PM	PM_SLP_S4_2_L	19 45 46
P118	PM	PM_SLP_S4_3_L	5 19
P39	PM	PM_SLP_S4_L	19 32
P43	PM	PM_SLP_S5_L	19 45
P41	PM	PM_SUS_PWR_ACK	19
P42	PM_VTT	PM_SYNC	11 19
P122	PM	SDCARD_PLT_RST_L	27 44
P45	PM	PM_SYSRST_L	19 27 45
P44	PM	PM_SYS_PWRGD	19 32 63
P46	PM_VTT	PM_THRMTRIP_L	11 21 46
P48	PM	RSMRST_PWRGD	45 63
P47	PM	RTC_RESET_L	18 91
P50	PM_VTT	CPU_PWRGD	11 21 25
P49	PM	CPU_RESET_L	11 27
P51	PM	PGOOD_1V05ME_G1	63
P53	PM	PGOOD_1V05ME_G2	63
P55	PM	PGOOD_1V8_S0_G1	63
P54	PM	PGOOD_1V8_S0_G2	63
P56	PM	PGOOD_CPU_GFX_DDR	63
P58	PM	PGOOD_P12V_S3	
P60	PM	PGOOD_P1V05_ME_S5	
P57	PM	PGOOD_P1V5_S0	72
P59	PM	PGOOD_P1V8_S0	63
P63	PM	PGOOD_P3V3_ME	72
P66	PM	PGOOD_P3V3_S0	48 63 72
P64	PM	PGOOD_P3V3_S3	44 72
P65	PM	PGOOD_P5V_S0	62 72
P61	PM	PGOOD_PCH_AND_P1V8	63
P62	PM	PGOOD_PCH_S0	63
P68	PM	PGOOD_SYSPWROK	63
P67	PM	PGOOD_SYSPWROK_R	63
P69	PM	RTC_RESET_L	18 91
P70	PM	P12V_S3_EN	62 72
P71	PM	P1V05_ME_SM_EN	62 72
P73	PM	P1V5_S0_EN	62 72
P72	PM	P3V3ME_EN	62 72
P74	PM	P3V3S0_EN	62 72
P75	PM	P3V3S3_EN	62 72
P76	PM	P5VS0_EN	62 72
P78	PM	P5VS3_EN	62 69
P77	PM	PCHCORE_REG_EN	62 68
P79	PM	PCHCORE_REG_PGOOD	5 62 63 68
P121	PM	PEG_RESET_L	9 27
P80	PM	SDCARD_RESET	21 25 44 92

	NET_TYPE		
	PHYSICAL	SPACING	
P82	PM	4V5_REG_EN	55
P81	PM	ALL_SYS_PWRGD_R	6 25 32 63
P84	PM	ALL_SYS_PWRGD_SMC	45 63
P83	PM	CK505_27MHZ_EN	26
P85	PM	CPUVTT_REG_EN	62 67
P86	PM_VTT	CPUVTT_REG_PGOOD	11 62 63 67
P87	PM	CPU_MEM_RESET_L	11 32
P88	PM	DDRVTT_EN	32 62 70
P89	PM	DEBUG_RESET_L	27 47
P90	PM	FWPHY_RESET_L	39
P91	PM	FWXIO_SNOOP_EN	39
P92	PM	FW_RESET_L	27 39
P93	PM	GFX_VR_EN	
P94	PM	GFX_VR_PGOOD	
P95	PM	LAN_RESET_L	27 36
P97	PM	MEM_RESET_L	30 31 32
P96	PM	MINI_RESET_L	27 33
P98	PM	SMC_DELAYED_PWRGD	46 63
P100	PM	SMC_LRESET_L	27 45
P102	PM	SMC_RESET_L	45 46 47
P103	PM	T28_RESET_L	
P104	PM_VTT	XDP_CPUPWRGD	11 25
P105	PM_VTT	XDP_DBRESET_L	11 25 27
P106	PM_VTT	XDP_PWRGD	25

NET PHYSICAL FOR NC NETS
REMOVE WHEN CHECKPLUS IS FIXED

	NET_TYPE			
	ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	PCIE GRAPHICS			
P150		PCIE_85D	PCIE	NC_PCIE_CLK100M_EXCARD_N
P149		PCIE_85D	PCIE	NC_PCIE_CLK100M_EXCARD_P
P142		PCIE_85D	PCIE	NC_PCIE_EXCARD_D2R_N
P140		PCIE_85D	PCIE	NC_PCIE_EXCARD_D2R_P
P139		PCIE_85D	PCIE	NC_PCIE_EXCARD_R2D_C_N
P141		PCIE_85D	PCIE	NC_PCIE_EXCARD_R2D_C_P
P152	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXCARD_N
P151	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXCARD_P
P135	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXTE_N
P133	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXTE_P
P136	NO_TEST=TRUE	USB_90D	USB	NC_USB_TPAD_N
P134	NO_TEST=TRUE	USB_90D	USB	NC_USB_TPAD_P

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PM RESETS ENABLES PGOOD CONST

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

	IN	PP5V_S3_CAMERA	FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
85 44	IN	USB_CAMERA_L_P	FUNC_TEST=TRUE
85 44	IN	USB_CAMERA_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
2 Ground Testpoints near J4700

J4750 USB CARD READER

85 44	IN	USB_SDCARD_L_P	FUNC_TEST=TRUE
85 44	IN	USB_SDCARD_L_N	FUNC_TEST=TRUE
91 44 25 21	IN	SDCARD_RESET	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4720 USB BLUETOOTH

85 44	IN	USB_BT_L_P	FUNC_TEST=TRUE
85 44	IN	USB_BT_L_N	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4720
2 Ground Testpoints near J4720

J4780 IR BOARD

85 44	IN	USB_IR_L_P	FUNC_TEST=TRUE
85 44	IN	USB_IR_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4780
2 Ground Testpoints near J4780

J4520 SATA ODD (HIGH SPEED)

84 42	IN	SATA_ODD_R2D_P	FUNC_TEST=TRUE
84 42	IN	SATA_ODD_R2D_N	FUNC_TEST=TRUE
84 42	IN	SATA_ODD_D2R_C_N	FUNC_TEST=TRUE
84 42	IN	SATA_ODD_D2R_C_P	FUNC_TEST=TRUE
45 42	IN	SMC_ODD_DETECT	FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
5 Ground Testpoints near J4520

J4510 SATA HDD (HIGH SPEED)

84 42	IN	SATA_HDD_R2D_P	FUNC_TEST=TRUE
84 42	IN	SATA_HDD_R2D_N	FUNC_TEST=TRUE
84 42	IN	SATA_HDD_D2R_C_N	FUNC_TEST=TRUE
84 42	IN	SATA_HDD_D2R_C_P	FUNC_TEST=TRUE

3 Ground Testpoints near J4510

J5520 ANALOG LCD TEMP SENSOR

88 51	IN	SNS_LCD_P	FUNC_TEST=TRUE
88 51	IN	SNS_LCD_N	FUNC_TEST=TRUE

J5521 AMBIENT TEMP SENSOR

88 51	IN	SNS_AMB_P	FUNC_TEST=TRUE
88 51	IN	SNS_AMB_N	FUNC_TEST=TRUE

J5551 ODD TEMP SENSOR

88 51	IN	SNS_ODD_P	FUNC_TEST=TRUE
88 51	IN	SNS_ODD_N	FUNC_TEST=TRUE

J5600 ODD FAN

52	IN	FAN_0_PWR_L	FUNC_TEST=TRUE
52	IN	FAN_TACH0_L	FUNC_TEST=TRUE
89 52	IN	PP12V_S0_FAN0_L	FUNC_TEST=TRUE
52	IN	FAN_0_GND	FUNC_TEST=TRUE

J5700 CPU FAN

53	IN	FAN_2_PWR_L	FUNC_TEST=TRUE
53	IN	FAN_TACH2_L	FUNC_TEST=TRUE
89 53	IN	PP12V_S0_FAN2_L	FUNC_TEST=TRUE
53	IN	FAN_2_GND	FUNC_TEST=TRUE

J5601 HD FAN

52	IN	FAN_1_PWR_L	FUNC_TEST=TRUE
52	IN	FAN_TACH1_L	FUNC_TEST=TRUE
89 52	IN	PP12V_S0_FAN1_L	FUNC_TEST=TRUE
52	IN	FAN_1_GND	FUNC_TEST=TRUE

J5550 HDD TEMP SENSOR

88 51	IN	HDD_OOB_TEMP_FILT	FUNC_TEST=TRUE

J5560 SKIN TEMP SENSOR

88 51	IN	SNS_SKIN_P	FUNC_TEST=TRUE
88 51	IN	SNS_SKIN_N	FUNC_TEST=TRUE

J6601 AUDIO MICROPHONE

59	IN	AUD_MIC_IN1_N_CONN	FUNC_TEST=TRUE
59	IN	GND_AUDIO_MIC1_CONN	FUNC_TEST=TRUE
59	IN	AUD_MIC_IN1_P_CONN	FUNC_TEST=TRUE

1 Ground Testpoint near J6601

J6602 AUDIO RIGHT SPEAKER

85 59 58	IN	AUD_SPKR_OUTLO2R_POUT	FUNC_TEST=TRUE
85 59 58	IN	AUD_SPKR_OUTLO2R_NOUT	FUNC_TEST=TRUE
85 59 57	IN	AUD_SPKR_OUTLO1R_POUT	FUNC_TEST=TRUE
85 59 57	IN	AUD_SPKR_OUTLO1R_NOUT	FUNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

85 59 58	IN	AUD_SPKR_OUTLO2L_POUT	FUNC_TEST=TRUE
85 59 58	IN	AUD_SPKR_OUTLO2L_NOUT	FUNC_TEST=TRUE
85 59 57	IN	AUD_SPKR_OUTLO1L_POUT	FUNC_TEST=TRUE
85 59 57	IN	AUD_SPKR_OUTLO1L_NOUT	FUNC_TEST=TRUE

		GND	16 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=16
89 6	IN	PP3V3_S3	2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
69 6	IN	PP5V_S3_REG	2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
89 6	IN	PP5V_S0	FUNC_TEST=TRUE MIN_ALLOWED_TPS=1

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